

BLE/BLED BLOCK DIAGRAM

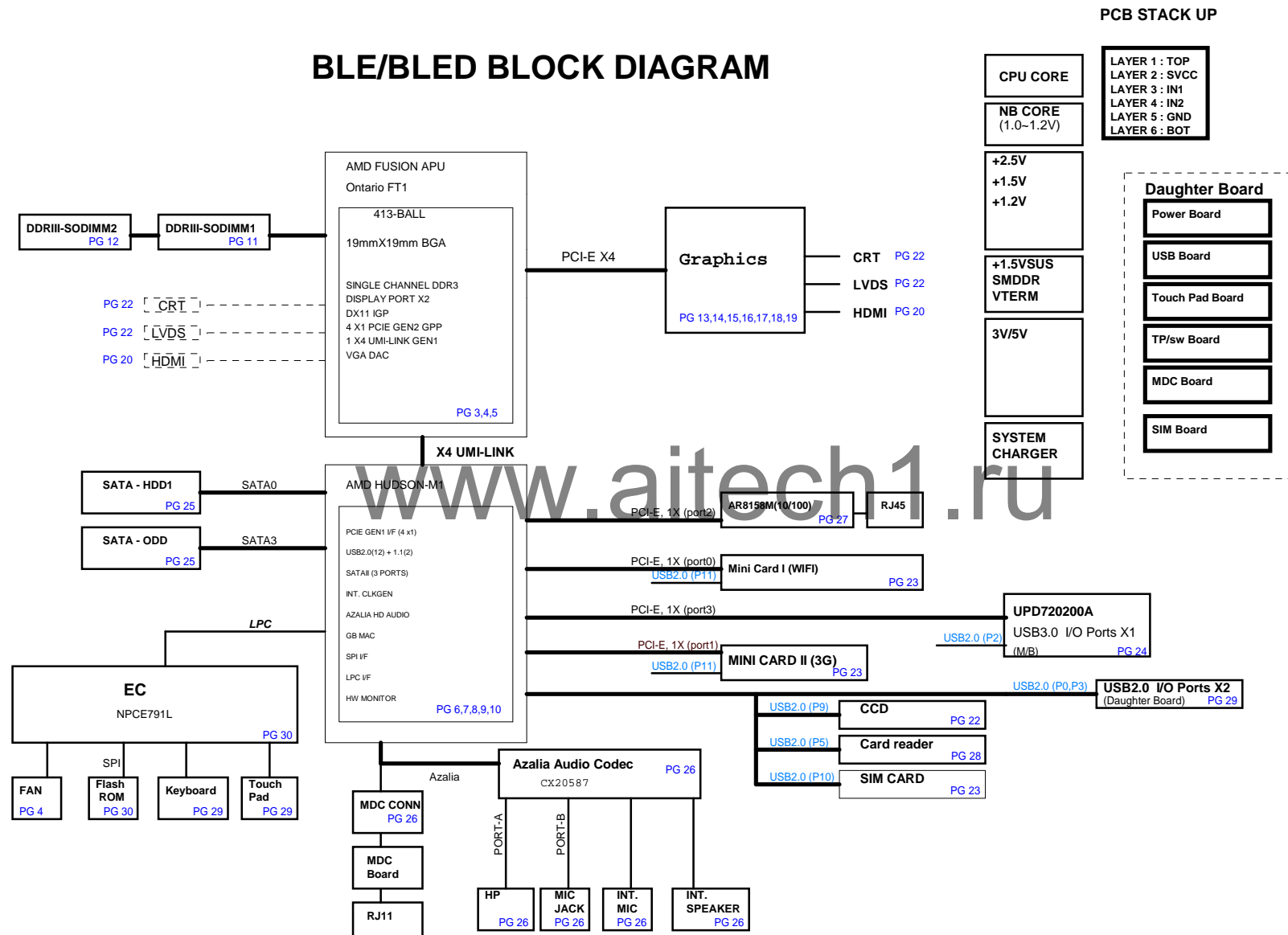






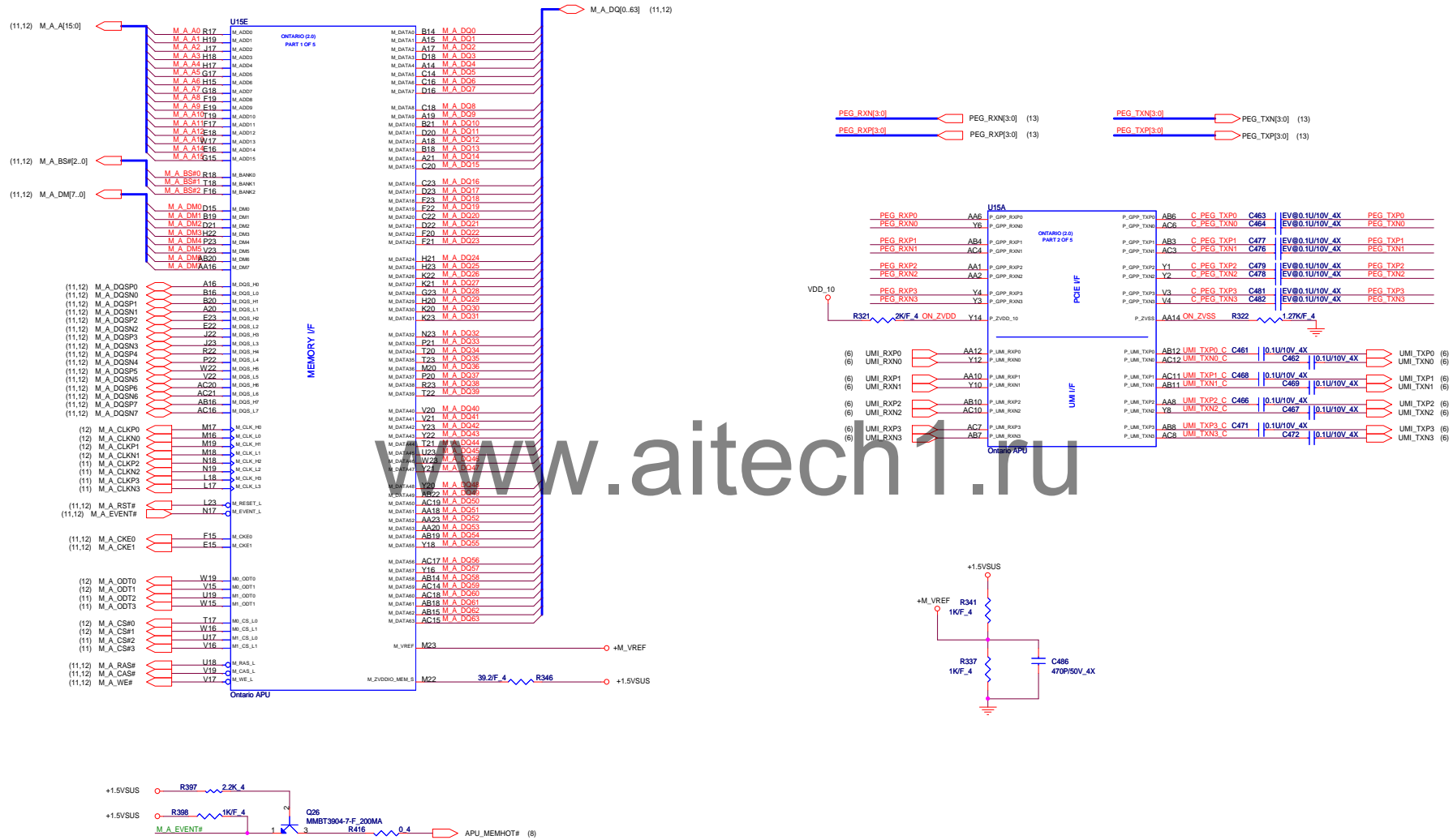


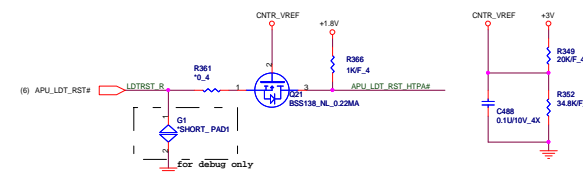
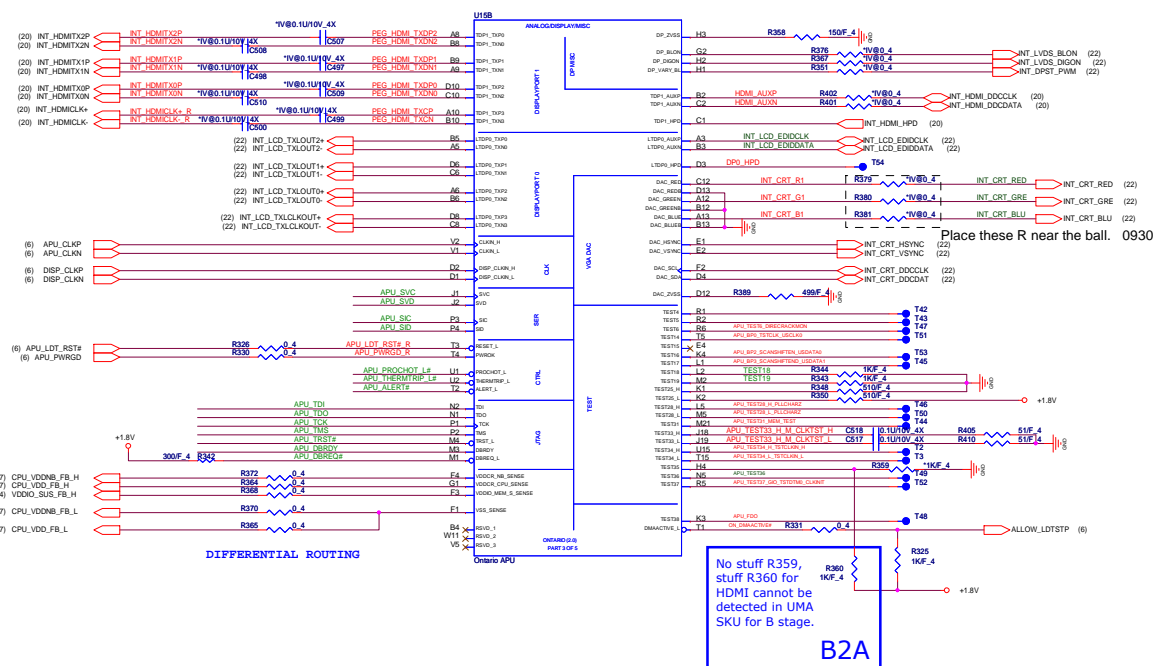
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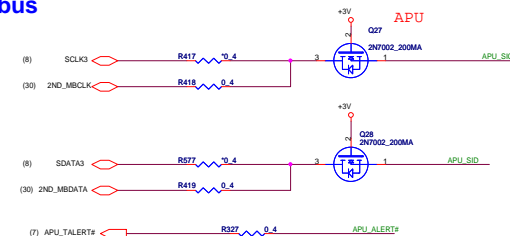
POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0-S5
+VCCRTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3V_3G	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5VPCU	+5V	AC/DC Insert enable	S0-S5
+5V_ODD	+5V	MAIN_ON	S0
WIMAX_P	+3.3V	WMAX_P for EC	
+1.1V	+1.1V	MAIN_ON	S0
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5VSUS	+1.5V	SUSON	S0-S5
+1.05V_USB3.0	+1.5V	SUSON	S0-S3
GPU_CORE	+1.1V	VRON	S0
CPU_CORE	+1.1V	MAIN_ON	S0
+1.1V_S5	+1.1V	S5ON	S0-S5
+VDDR	+0.9V	VRON	S0
+GPU_CORE	+1.0V	GPU_VRON	S0

GND PLANE	PAGE
 GND_SIGNAL	5
 AGND_+1.5V_SUS	34
 AGND_DC/DC	33
 Audio_GND	26
 ShieldGND	22
 GND	ALL

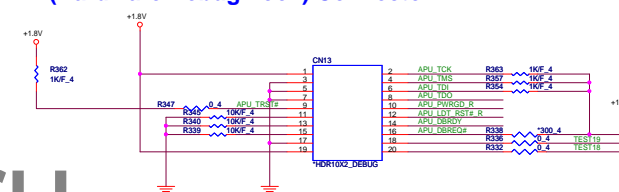




SMbus

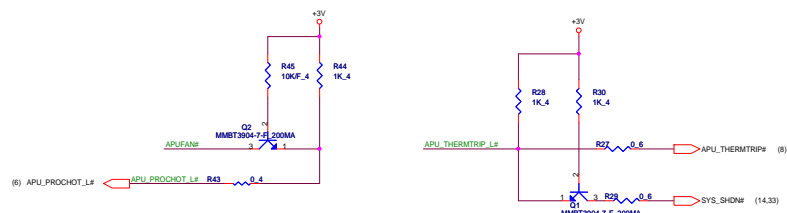


HDT(Hardware Debug Tool) Connector

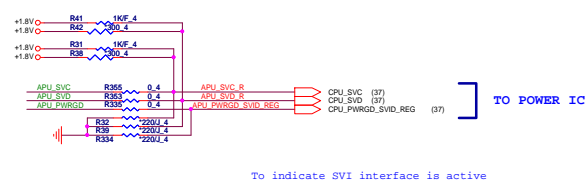


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Thermal Management Signals

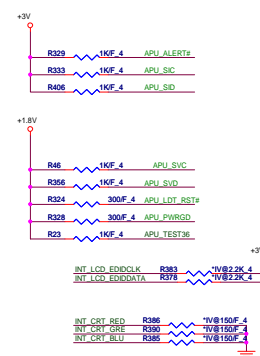
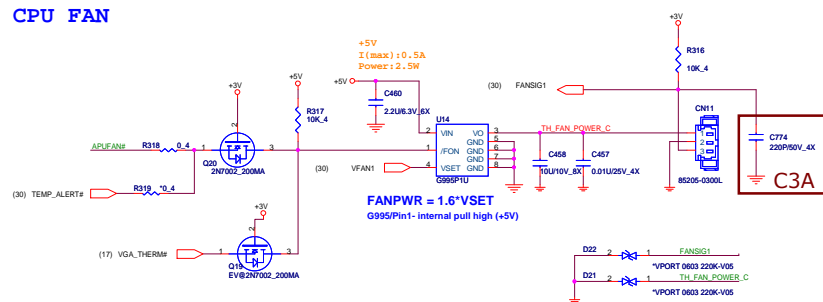


Serial VID

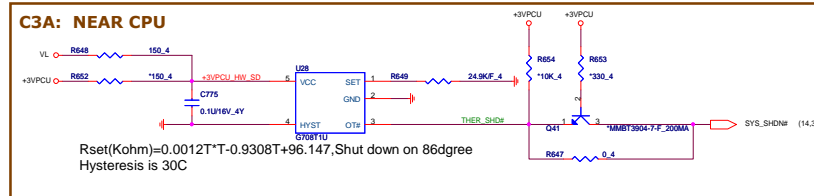


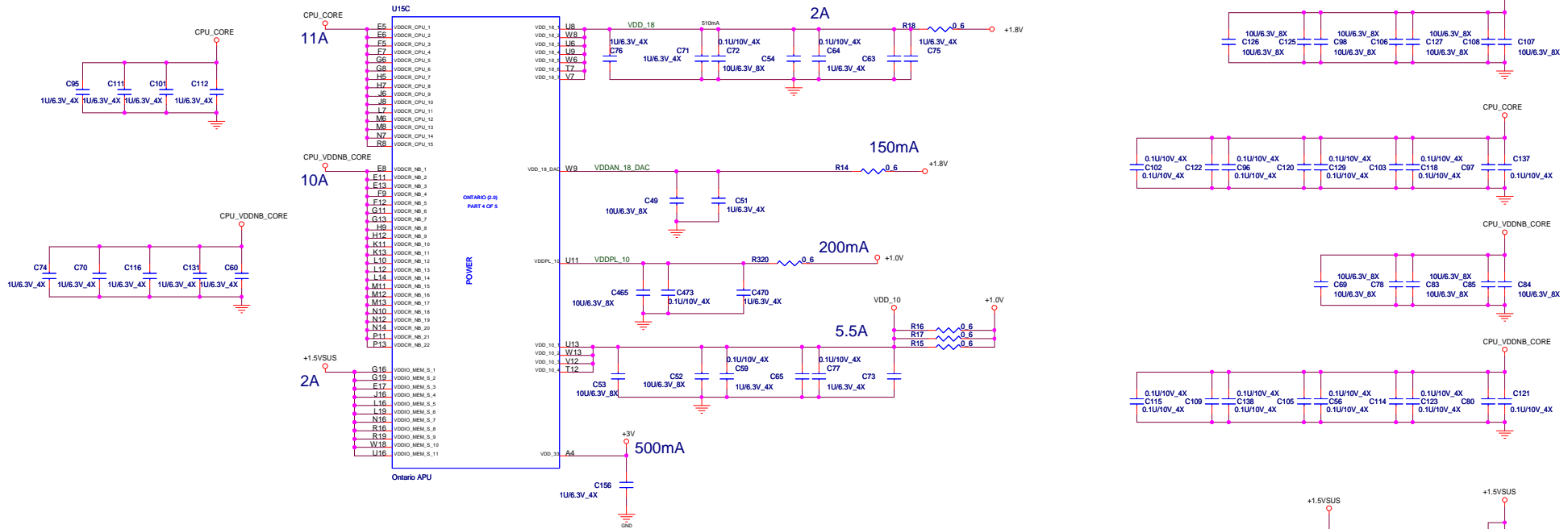
VFIX MODE		VID Override Circuit
SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

CPU FAN

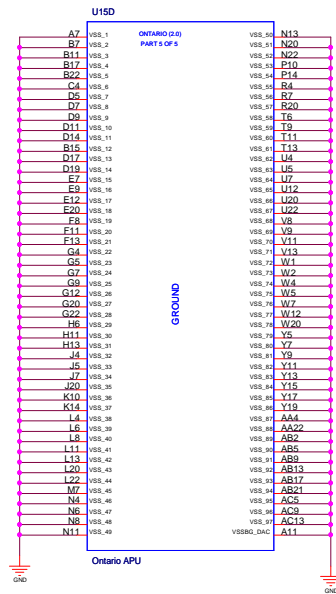


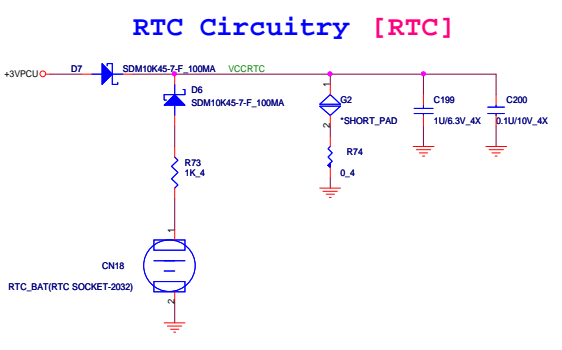
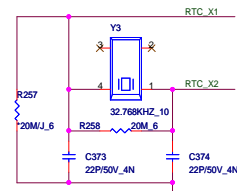
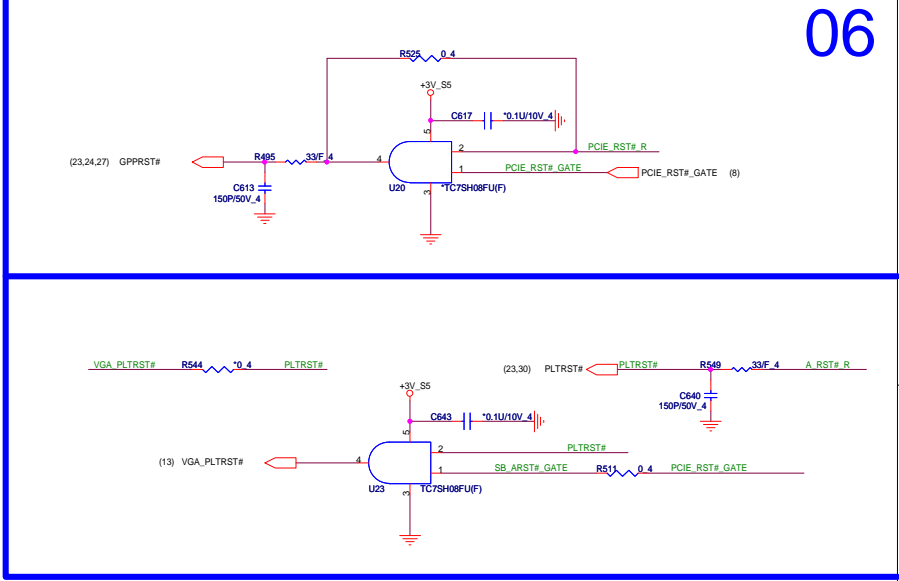
C3A: NEAR CPU



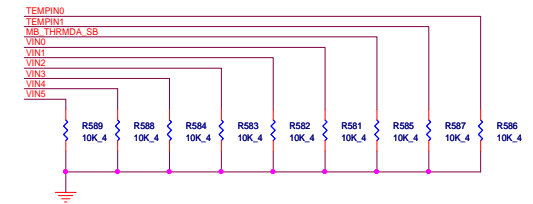
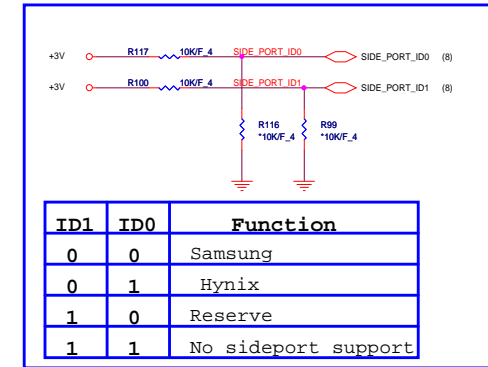
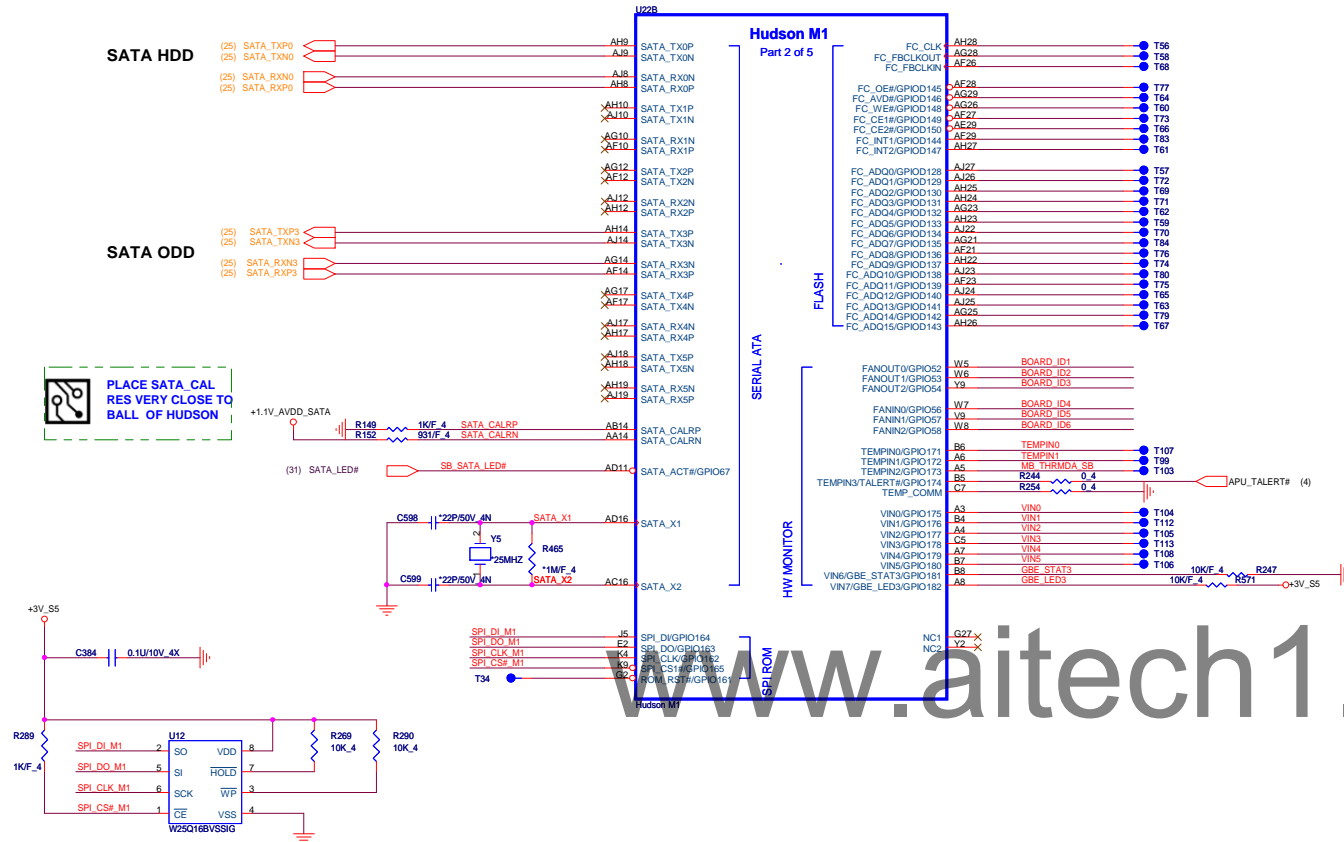


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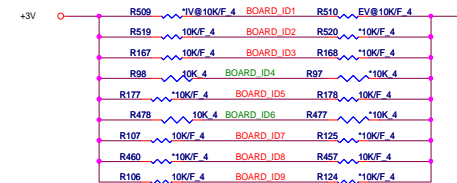


INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT)



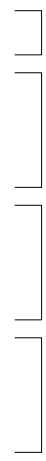
BOARD ID SETTING

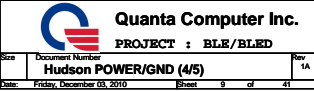
Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9
UMA SKU VGA SKU	H	L							
W/ MDC W/O MDC		H	L						
W/ HDMI W/O HDMI			H	L					
W/O 3G W/ 3G				H	L				
15" 14"					H	L			
W/O BT W/ BT						H	L		
13W 17W							H	L	
W/ CF W/O CF								H	L
W/O KB P W/ KB P									H

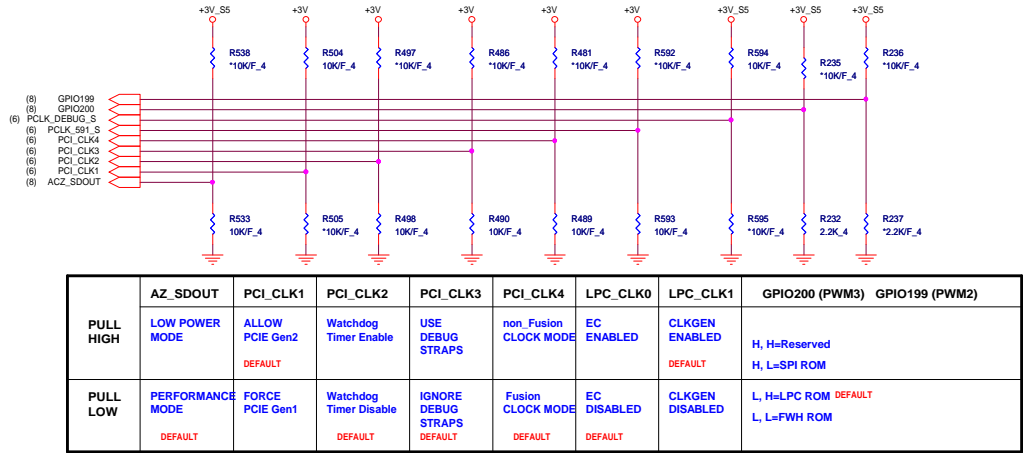


- (8) BOARD_ID7 BOARD_ID7
- (8) BOARD_ID8 BOARD_ID8
- (8) BOARD_ID9 BOARD_ID9

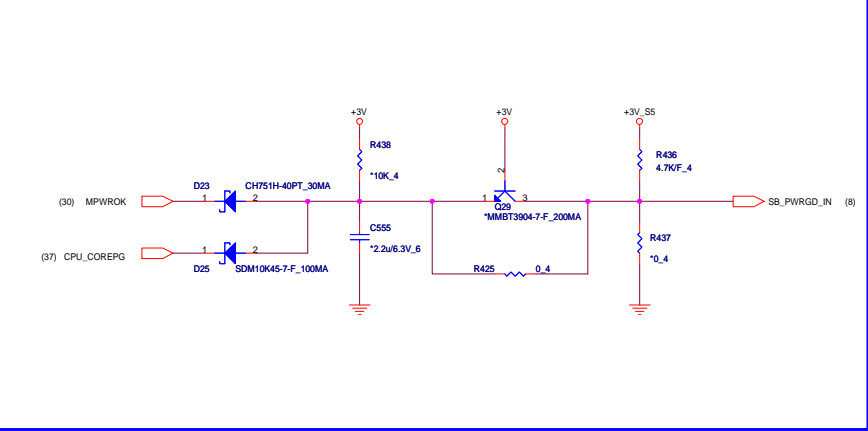
BOARD_ID4 CPU_SB# (23)





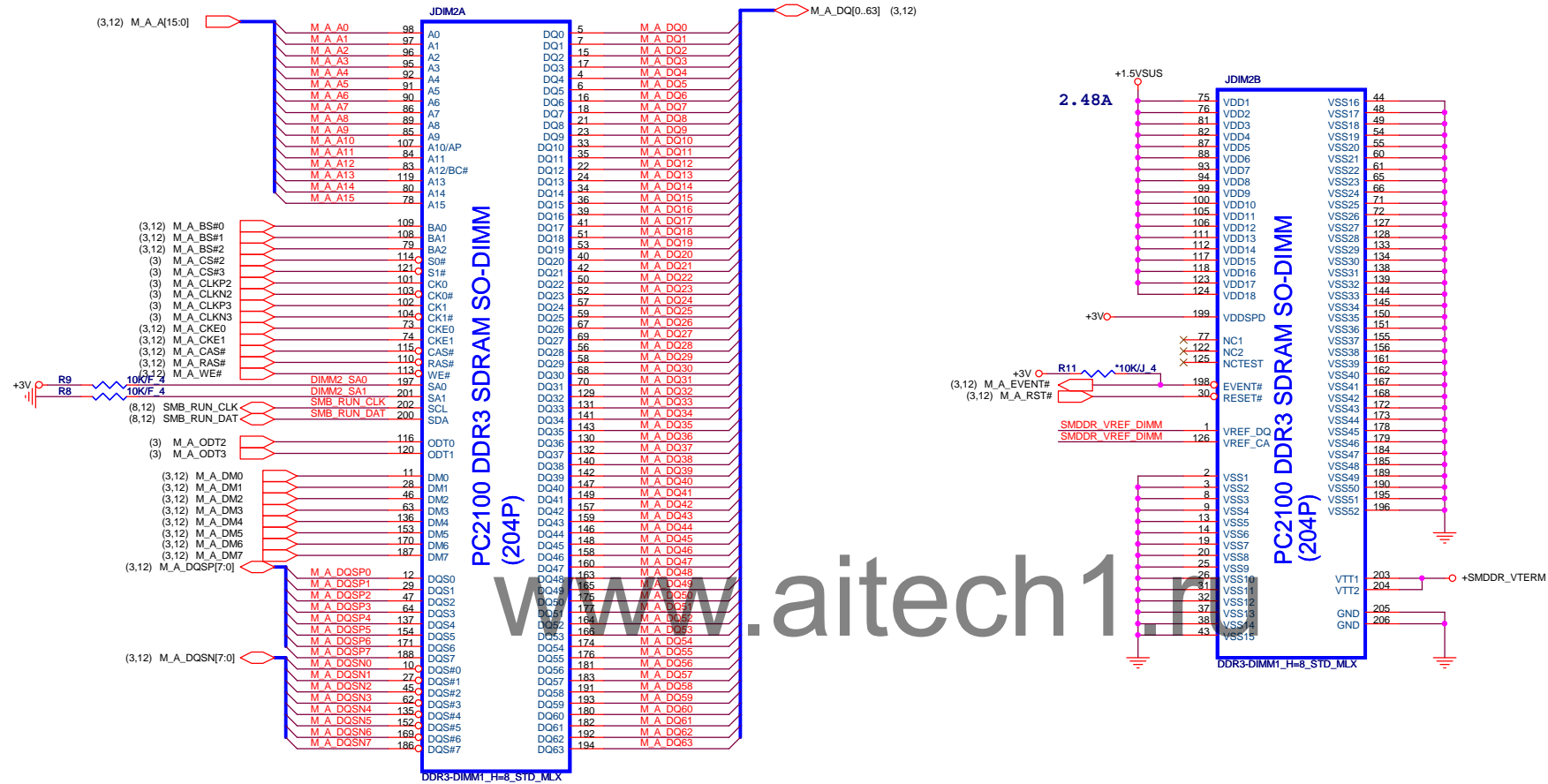


FCH POWER GOOD CIRCUIT

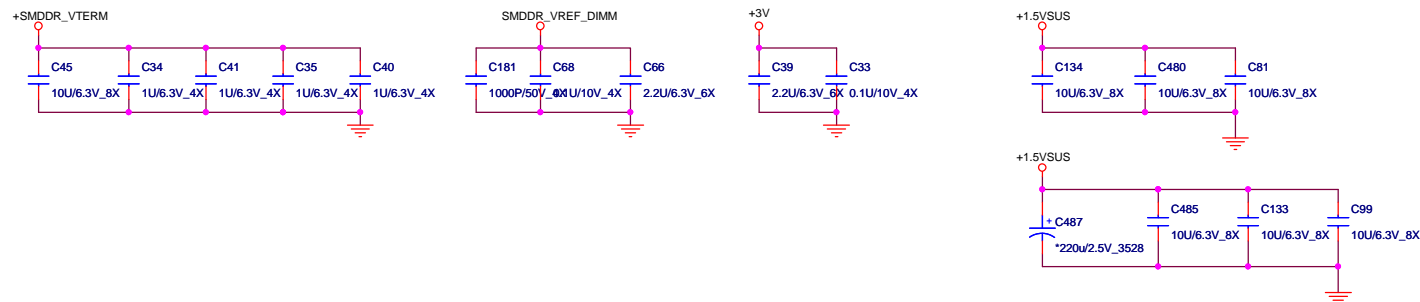


DEBUG STRAPS

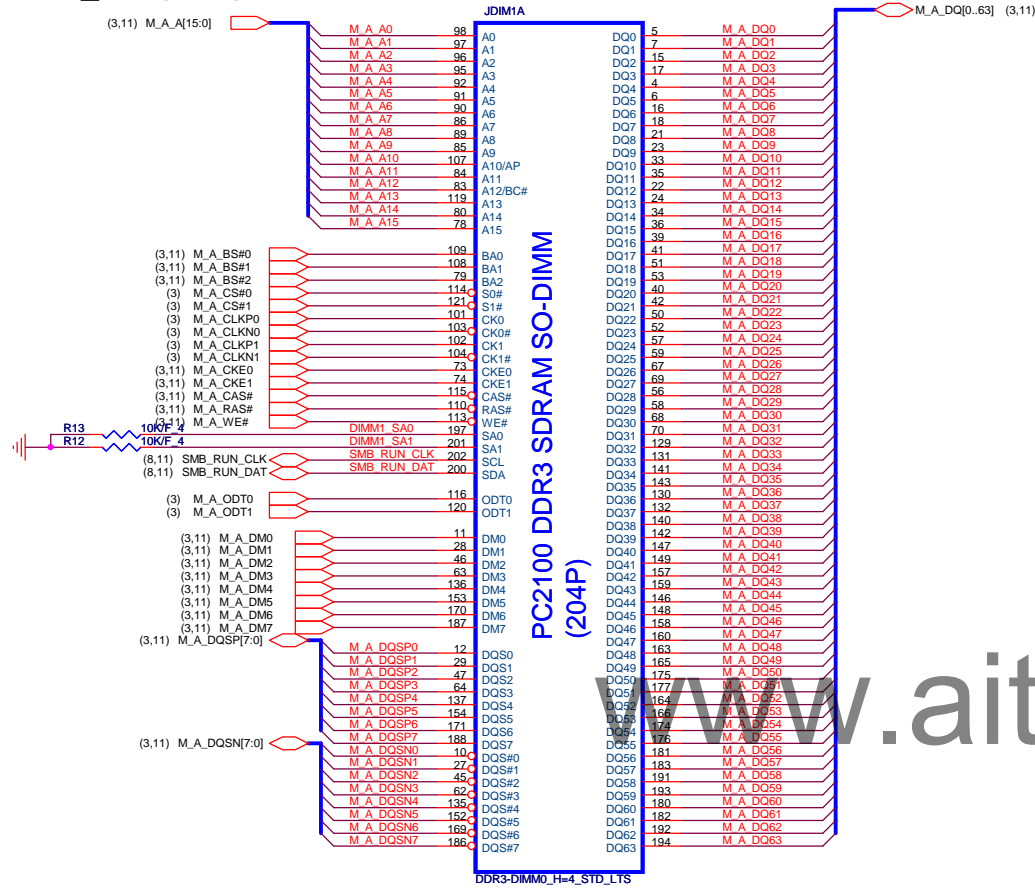
Ball Name	Strap Name	Default	Description	Setting
AD23	PCI_ROM_BOOT	1	0 -- Enable PCI MEM Boot 1 -- Disable PCI MEM Boot	(6) AD23
AD24	PCIE_EEPROM	1	0 -- Enable EEPROM 1 -- Disable EEPROM	(6) AD24
AD25	REFCLK Termination	1	0 -- Inverted REFCLK 1 -- Normal REFCLK	(6) AD25
AD26	AUTORUN_ILA	1	0 -- Enable ILA 1 -- Disable ILA	(6) AD26
AD27	PciPl1Byp	1	0 -- ByPass Int PLL 1 -- Int. PLL	(6) AD27
HUDSON_M1 HAS 15K INTERNAL PU FOR PCL_AD[27:23]				



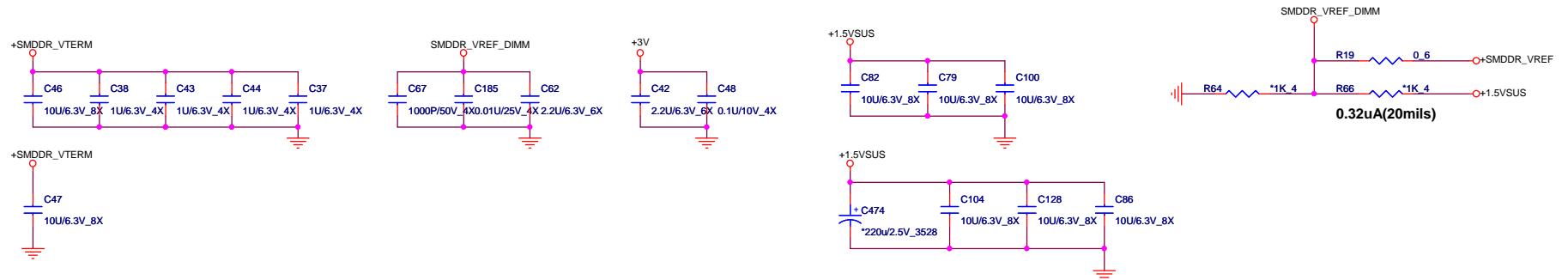
9.12A(VCC plane from source)

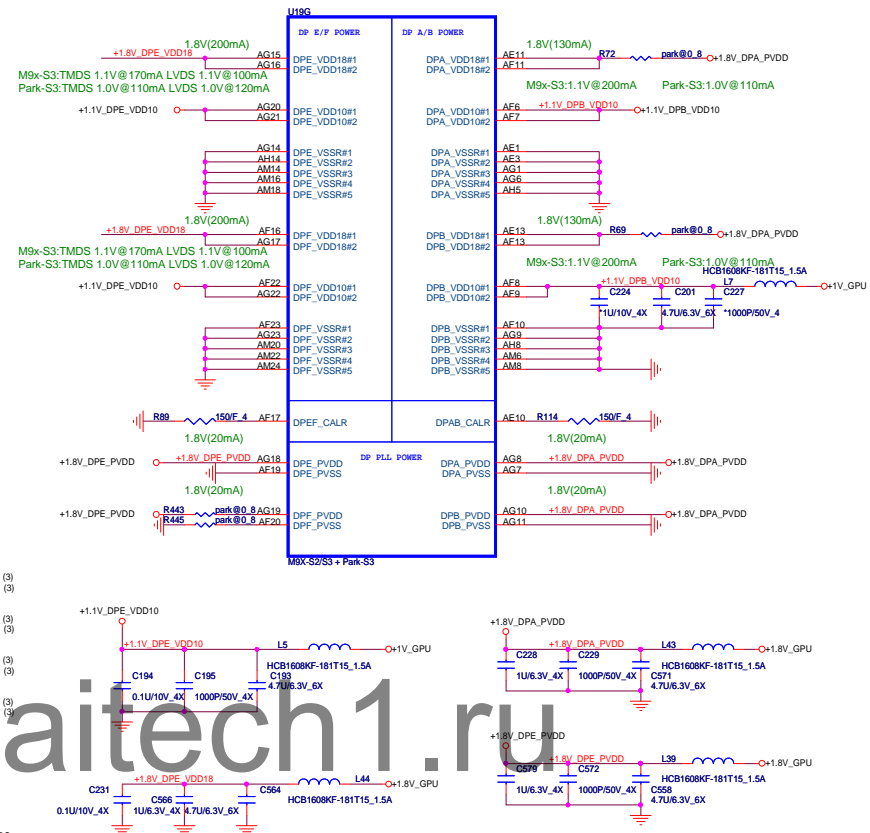
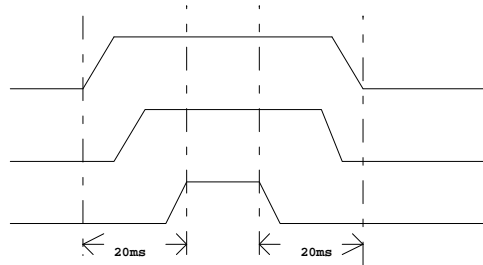


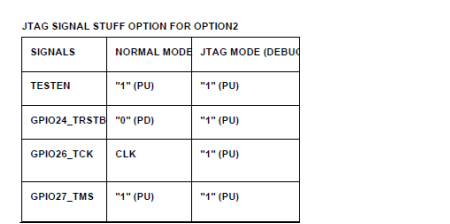
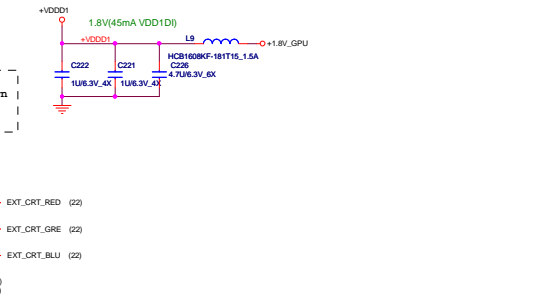
DDR_STD (DDR)

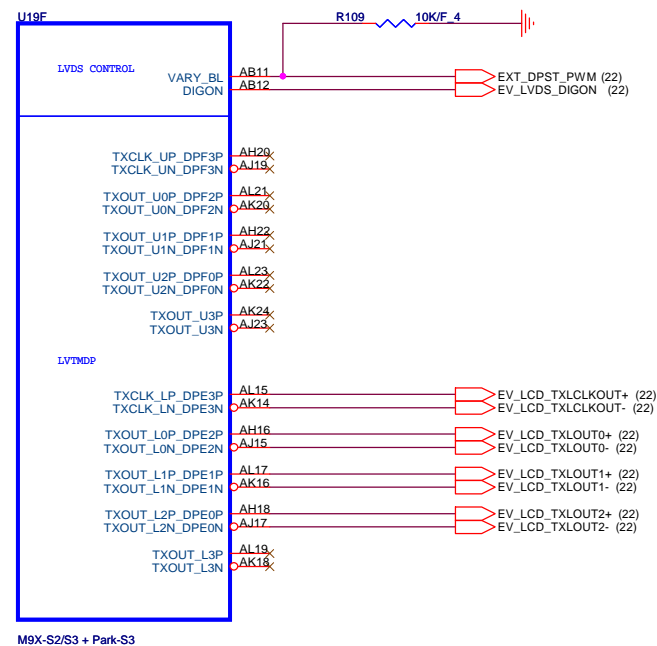
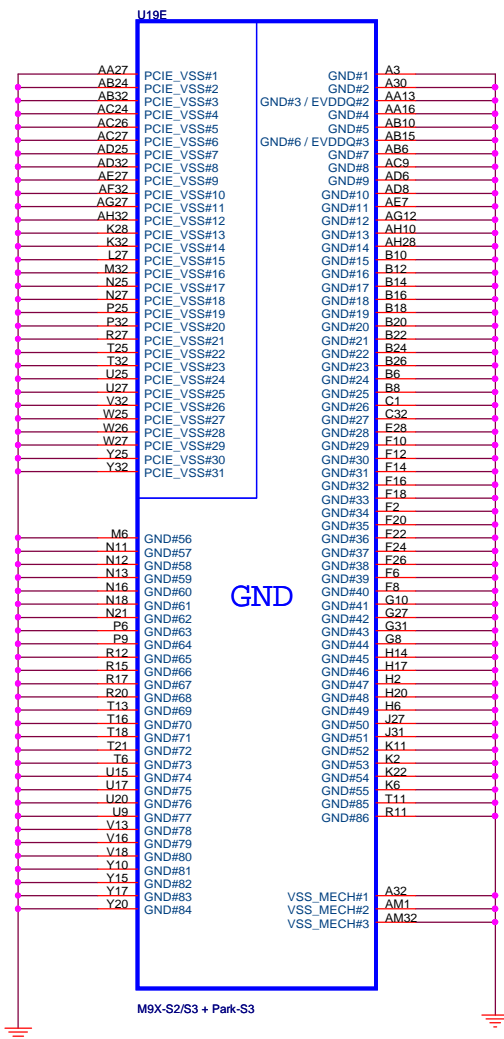


9.12A(VCC plane from source)









Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	PCI Express Full TX Output Swing 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
RSVD	GPIO8	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0 0 0
BIF_VGA_DIS	GPIO9		
RSVD	GPIO21		
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	1
AUD[0] AUD(1)	VSYN HSYN	AUD[1] AUD[0] 00 No Audio function 01 Audio for DisplayPort and HDMI if dongle is detected 10 Audio for DisplayPort only 11 Audio for both DisplayPort and HDMI	1 1
VIP_DEVICE_STRAP_ENA	V2SYN	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
RSVD	GENERIC		0

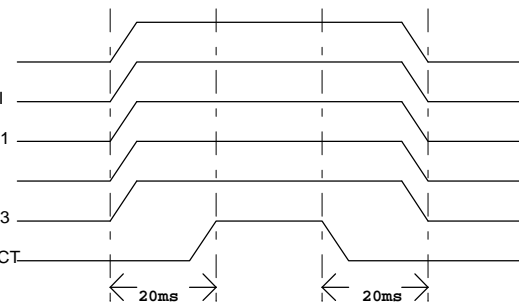
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Power Up/Down Sequence

GPU Power-on sequence

- 1 => +3V_DELAY
- 2 => +VGPU_CORE
- 3 => +VGPU_IO
- 4 => +1V_GPU
- 5 => +1.5V_GPU
- 6 => +1.8V_GPU
- 7 => dGPU_PWROK

+VGPU_CORE VDDC
+VGPU_IO VDDCI
+1.5V_GFX VDDR1
+1.0V_GFX IO
+3V_DELAY VDDR3
+1.8V_GFX VDD_CT

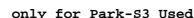


Quanta Computer Inc.

PROJECT : BLE/BLED

Size	Document Number	Rev
	Park-S3 LVDS/Straps(3/6)	1A

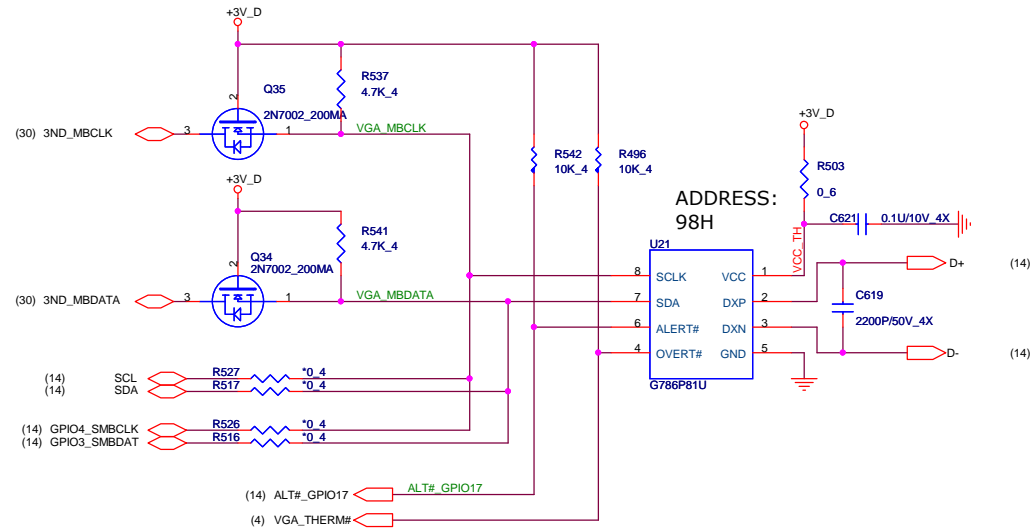
Date: Friday, December 03, 2010 Sheet 15 of 41



Park-S3 no support Back Bias

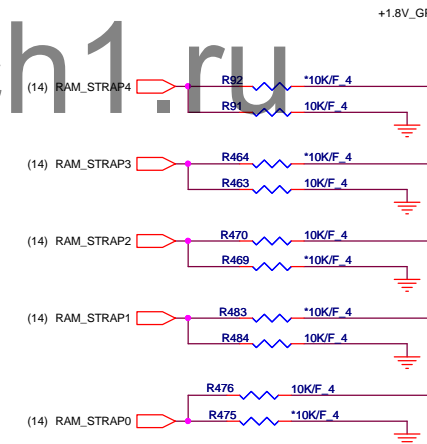
+VGPU_CORE L17
HCB1608KF-181T15 1.5A

Thermal Sensor

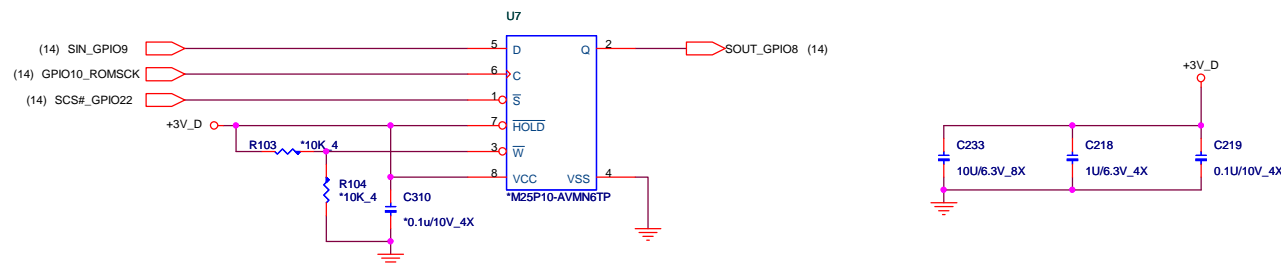


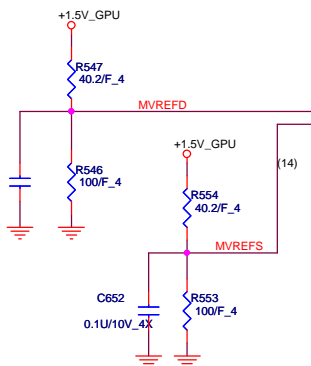
VRAM Memory TYPE

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	RAM_STRAP4 15"	RAM_STRAP4 14"
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW00 (64M*16)	512MB	0	1	0	0	0	1
			1GB	0	0	0	0	0	1
		AKD5MGGTW00	2GB	0	0	1	0	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT502 (64M*16)	512MB	0	1	0	1	0	1
			1GB	0	0	0	1	0	1
	K4W2G1646B-HC12	AKD5MGGT501	2GB	0	0	1	1	0	1



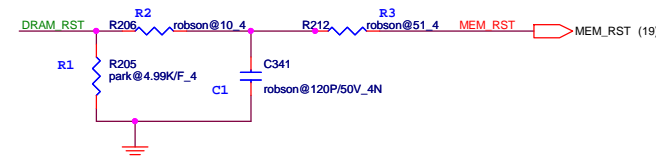
EEPROM





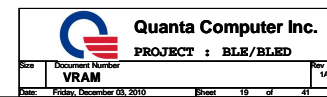
MEMORY INTERFACE

```
for Park-S3:Use only
for M9x-S3: no support
```

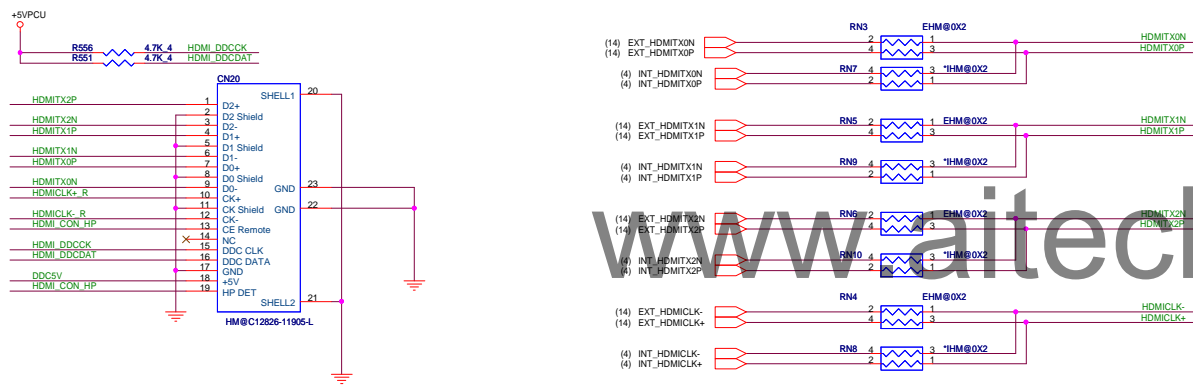
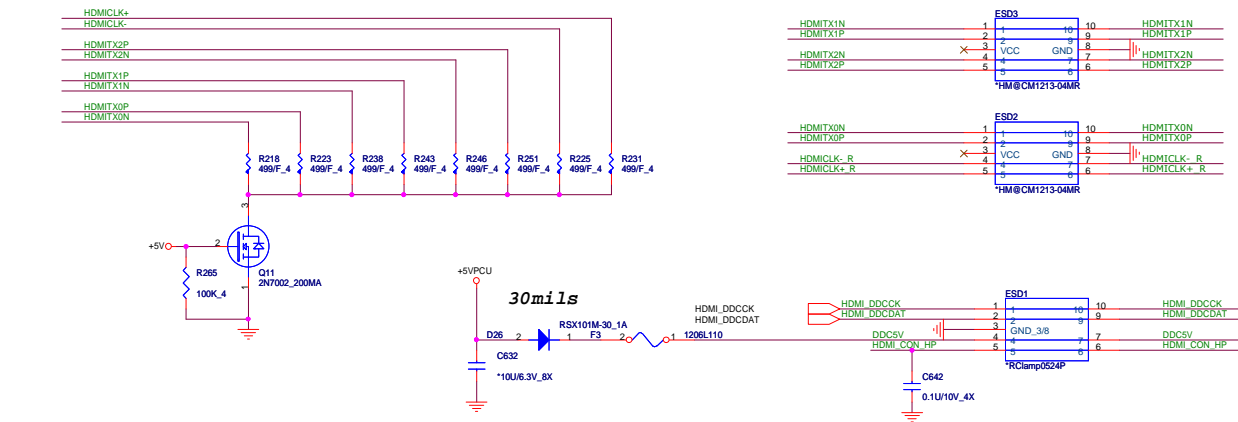


	M9x-S2/S3	Park-S3	Robson-S3
MEM_CALRN0(J25) MEM_CALRP0(K25)	NC	240R	240R
MEM_CALRP1(J8)	240R	150R	240R
TESTEN2#2(K7)	NC	0R	
R1	NC	10K	5K
R2	0R	680R	10R
R3	2.2K	NC	51R
C1	2.2nF	68pF	120pF

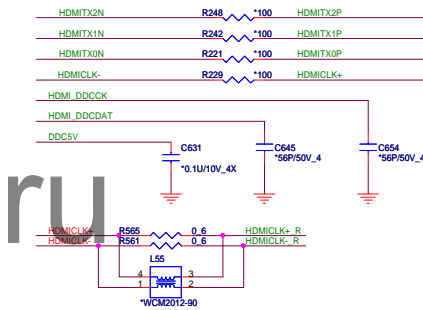
```
for Park-S3:Use Cap
0.1uF, Res 51.1R
Routing 50ohms
single-ended/100ohms
diff
```



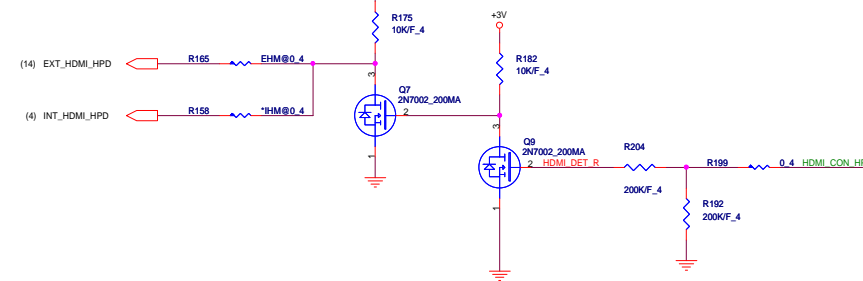
HDMI Conn [HDM]

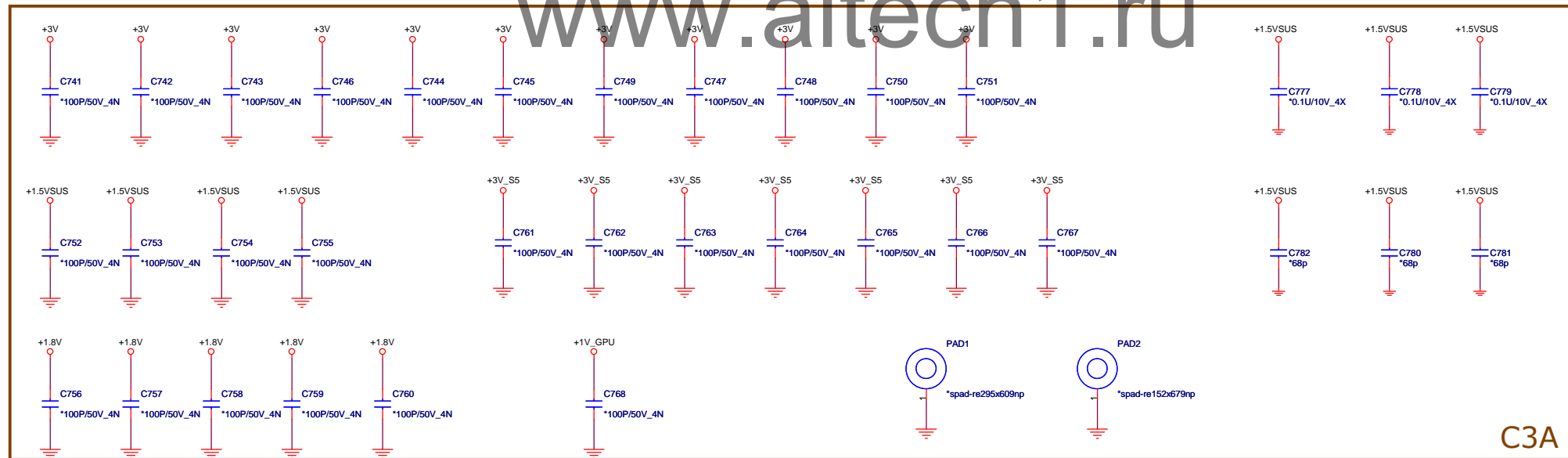
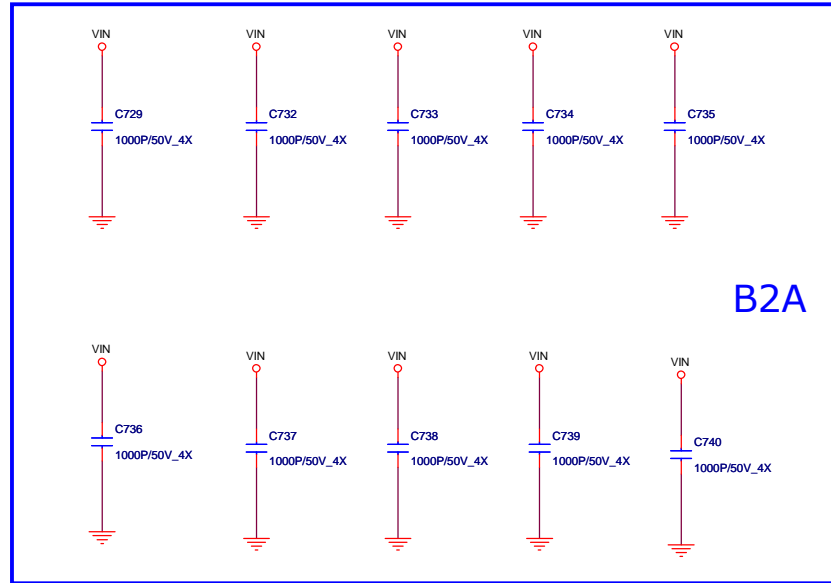
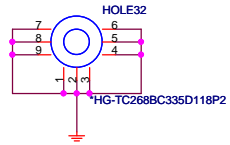
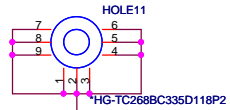


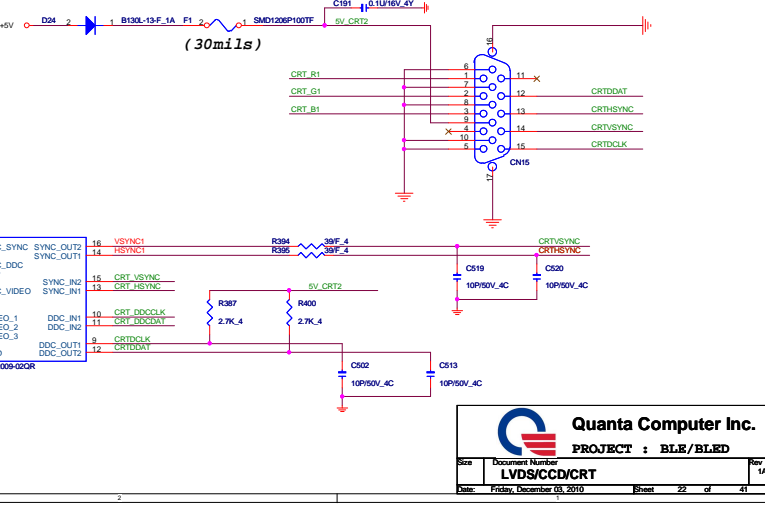
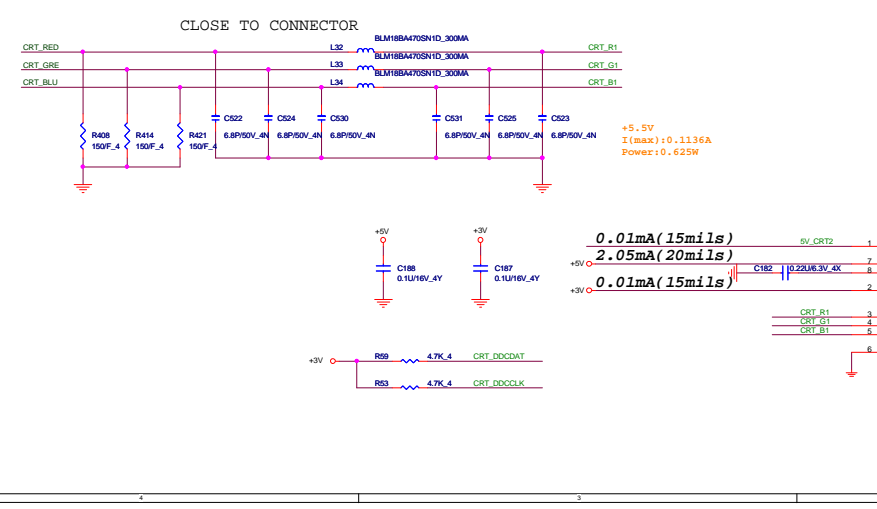
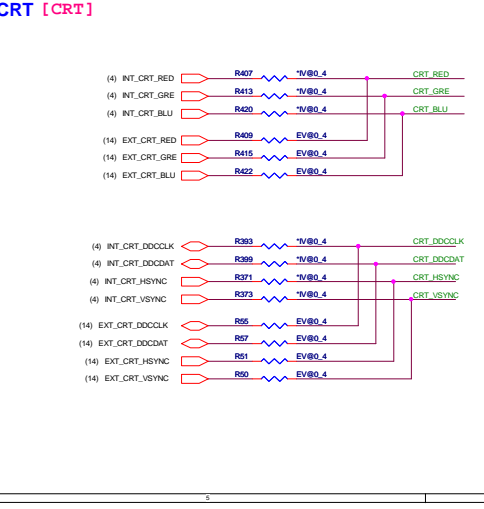
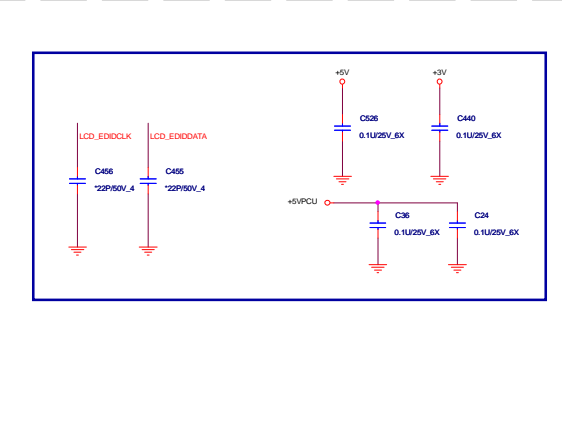
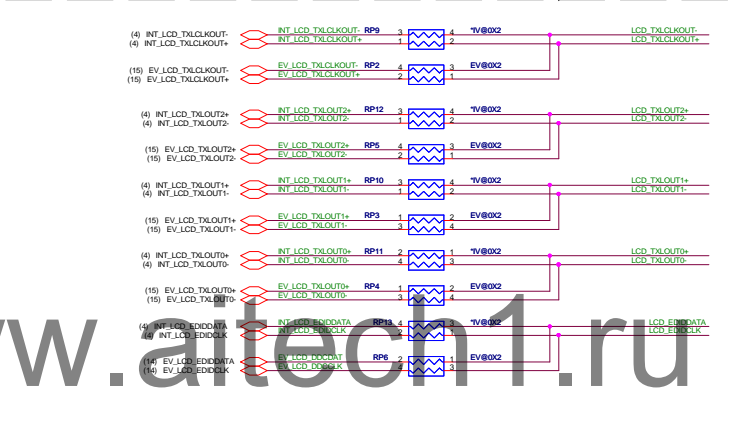
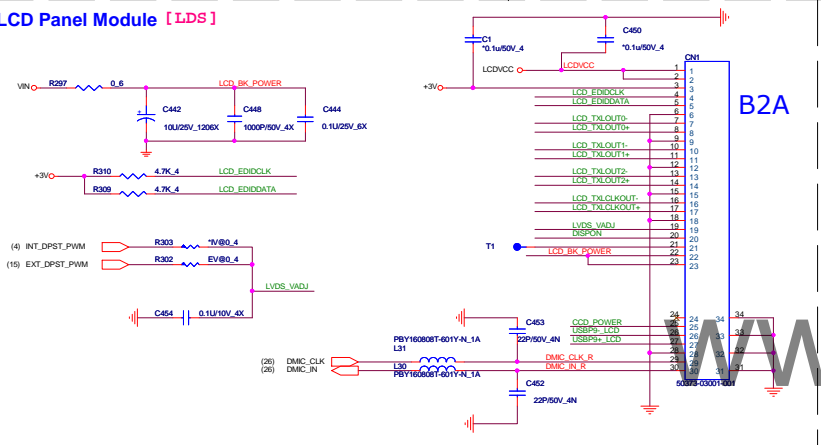
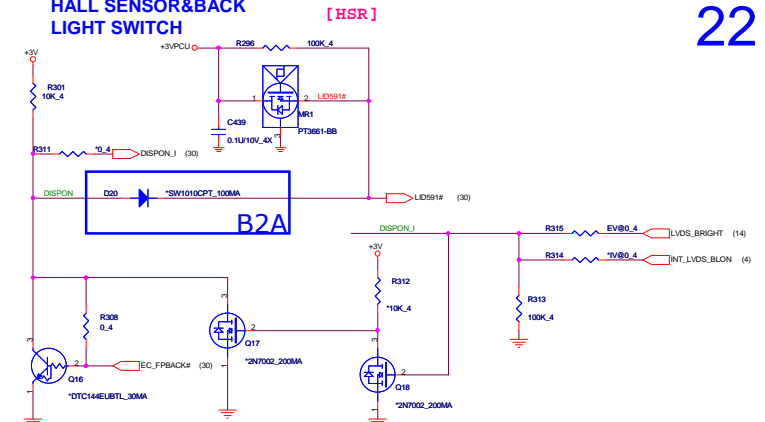
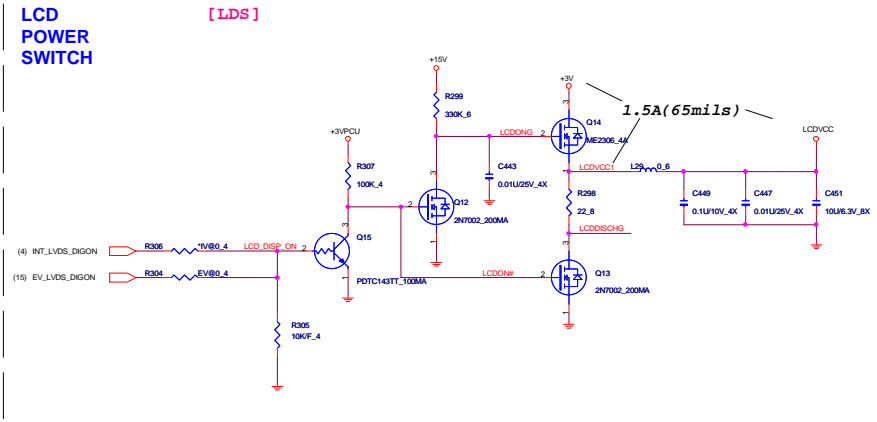
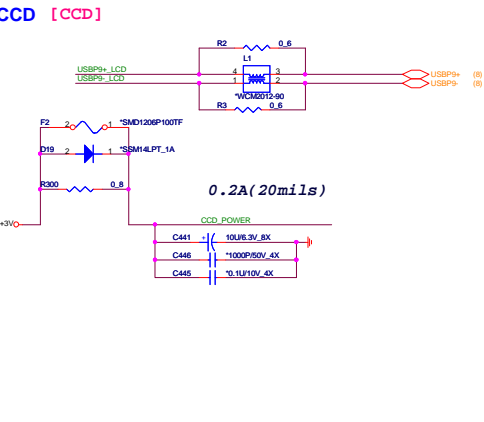
FOR EMI



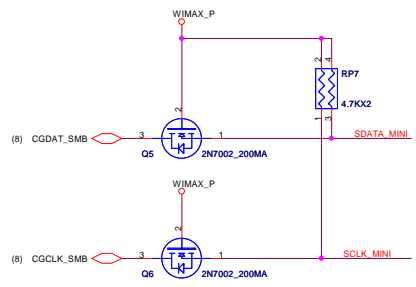
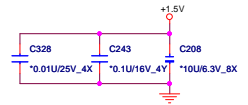
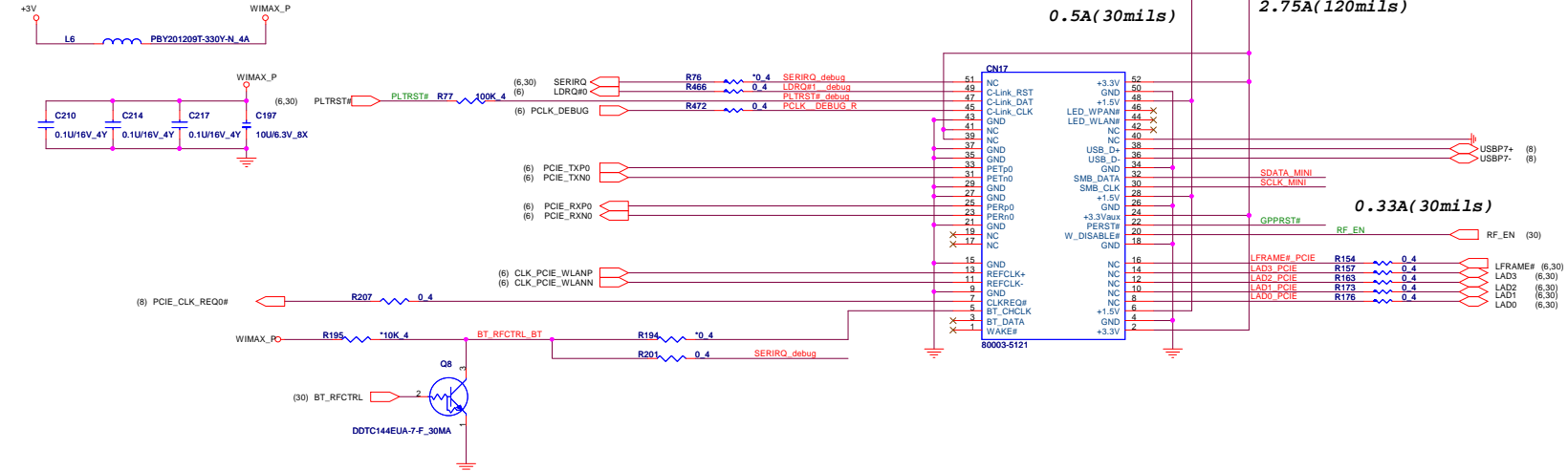
HDMI HPD SENSE



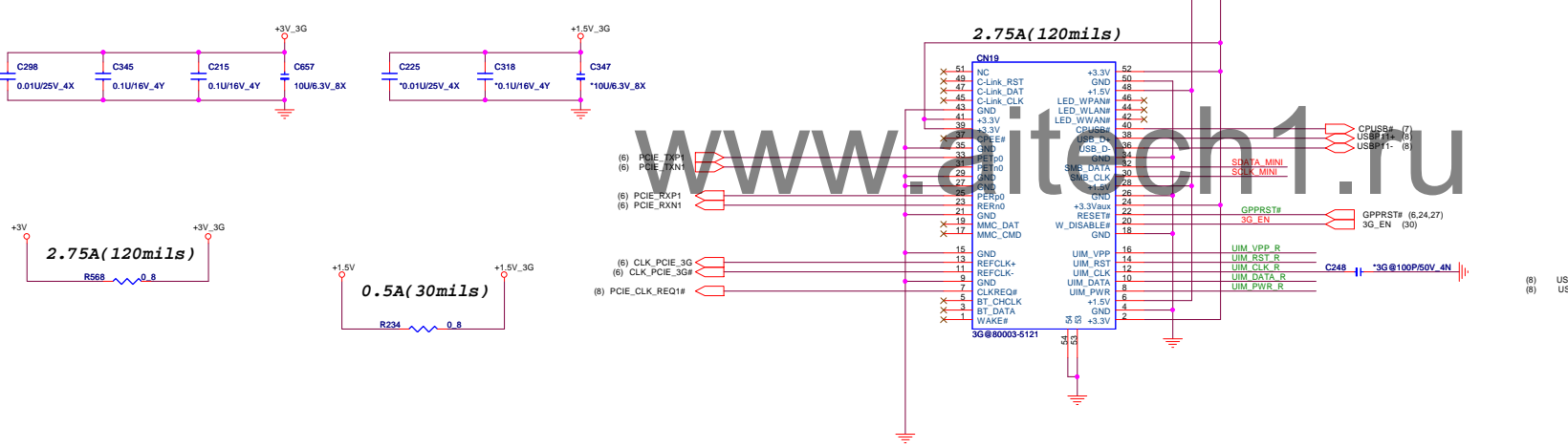




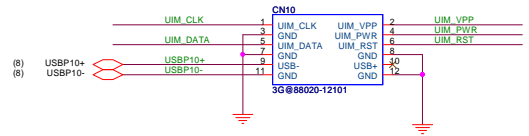
MINI Card Slot#1
(WiFi)



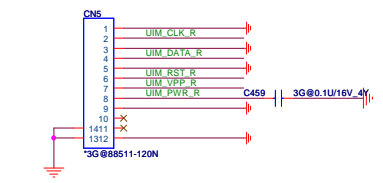
MINI Card Slot#2
3G



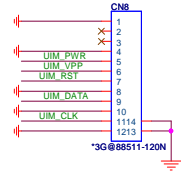
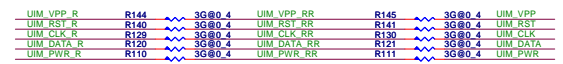
SIM CARD board to board



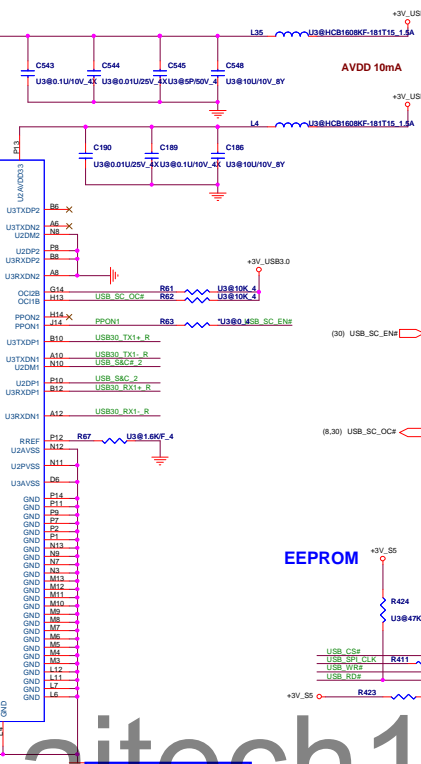
3G CONN



Close to 3G MINI Card



<U3B>



AVDD 10mA

+3V_USB3.0

USB3HCR1609KF-181T15_1.5A

+3V_USB3.0

USB3HCR1609KF-181T15_1.5A

USB Power switch

+5VPCU

USB

IN1 OUT1

IN2 OUT2

GND GND

G647E2P81U

+5VSUS_USBPO

C209 470P50V_4K

C196 0.1U10V_4K

C203 100U6.3V_3528P_E405

C205 10U6.3V_BX

C204 10U6.3V_BX

R75 470F_4

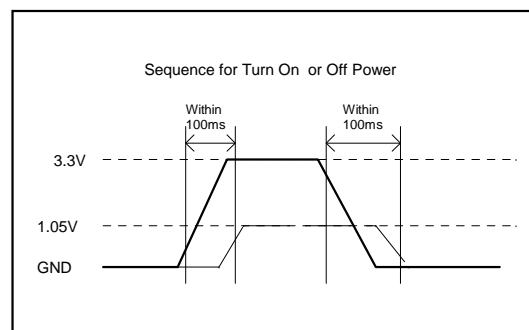
D4 2N7002_100MA

(D3) USB_SC_EN# USB_SC_EN#

(B36) USB_SC_OC# USB_SC_OC#

USB w S&C MAXIM solution <SLC>

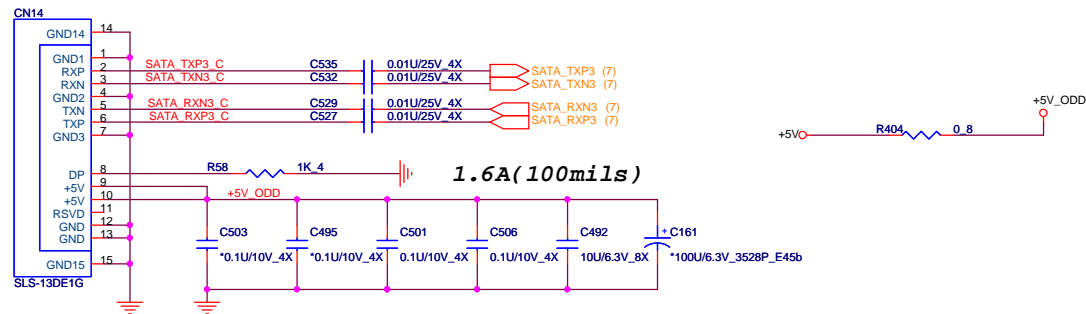
CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM



CB0	CB1	Status
0	0	Auto mode
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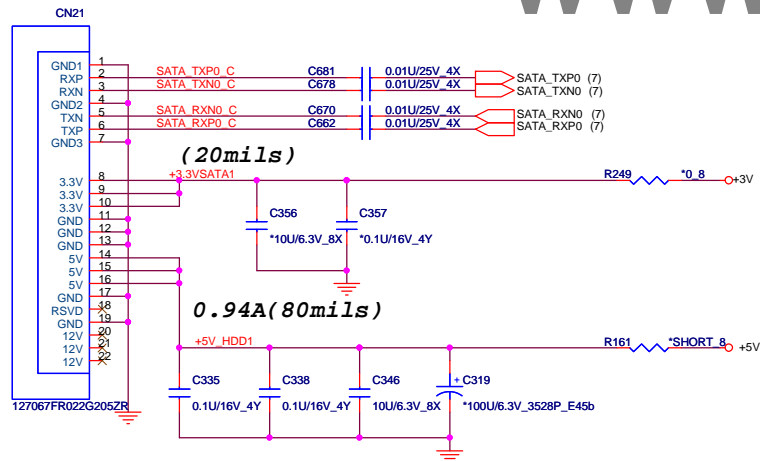
SATA ODD

[ODD]

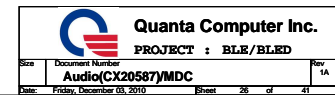


SATA HDD

[HDD]

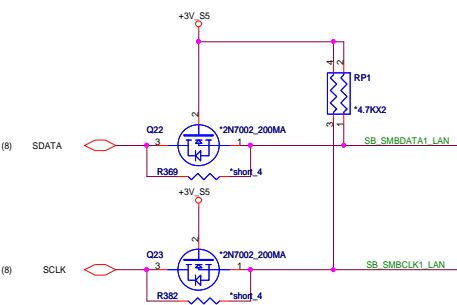
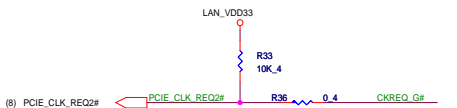
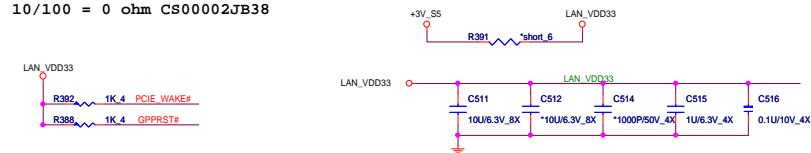


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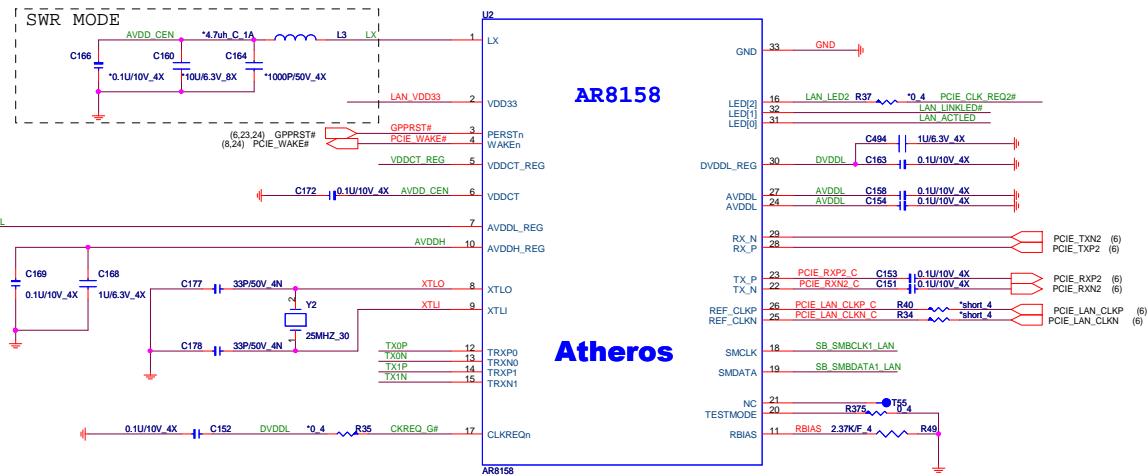
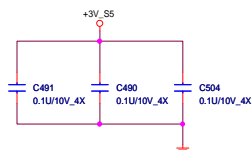
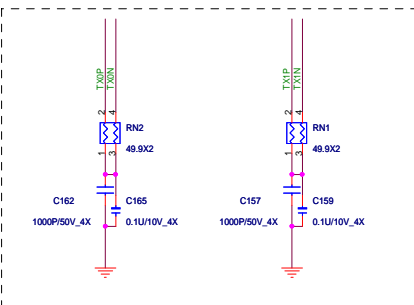


Atheros Lan AR5158

10/100 = 0 ohm CS00002JB38

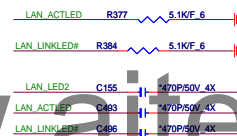


PLACE NEAR LAN IC SIDE



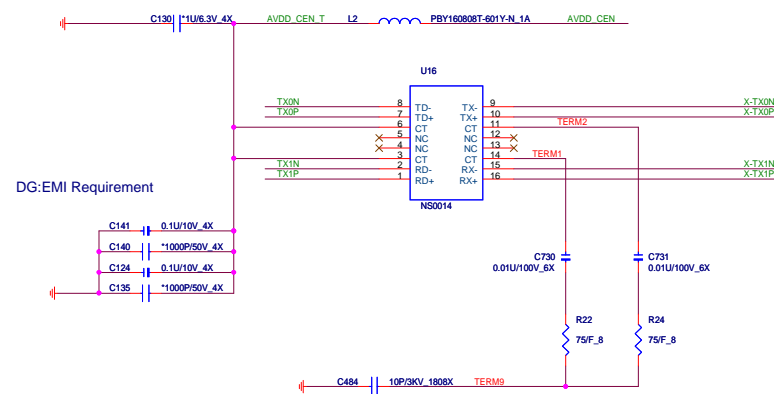
AMD 10/100: AR8158-BL1A-R = AL008158001

Power on Strapping pin

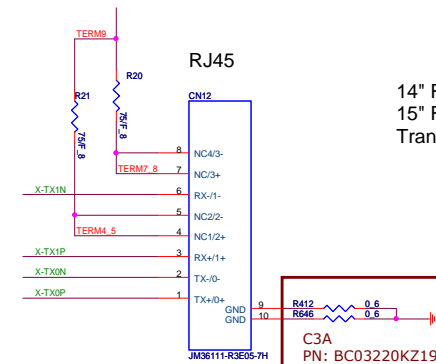


LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low

TRANSFORMER

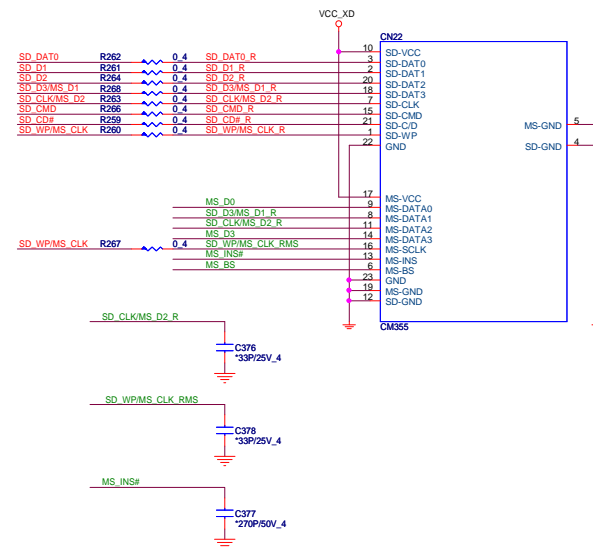
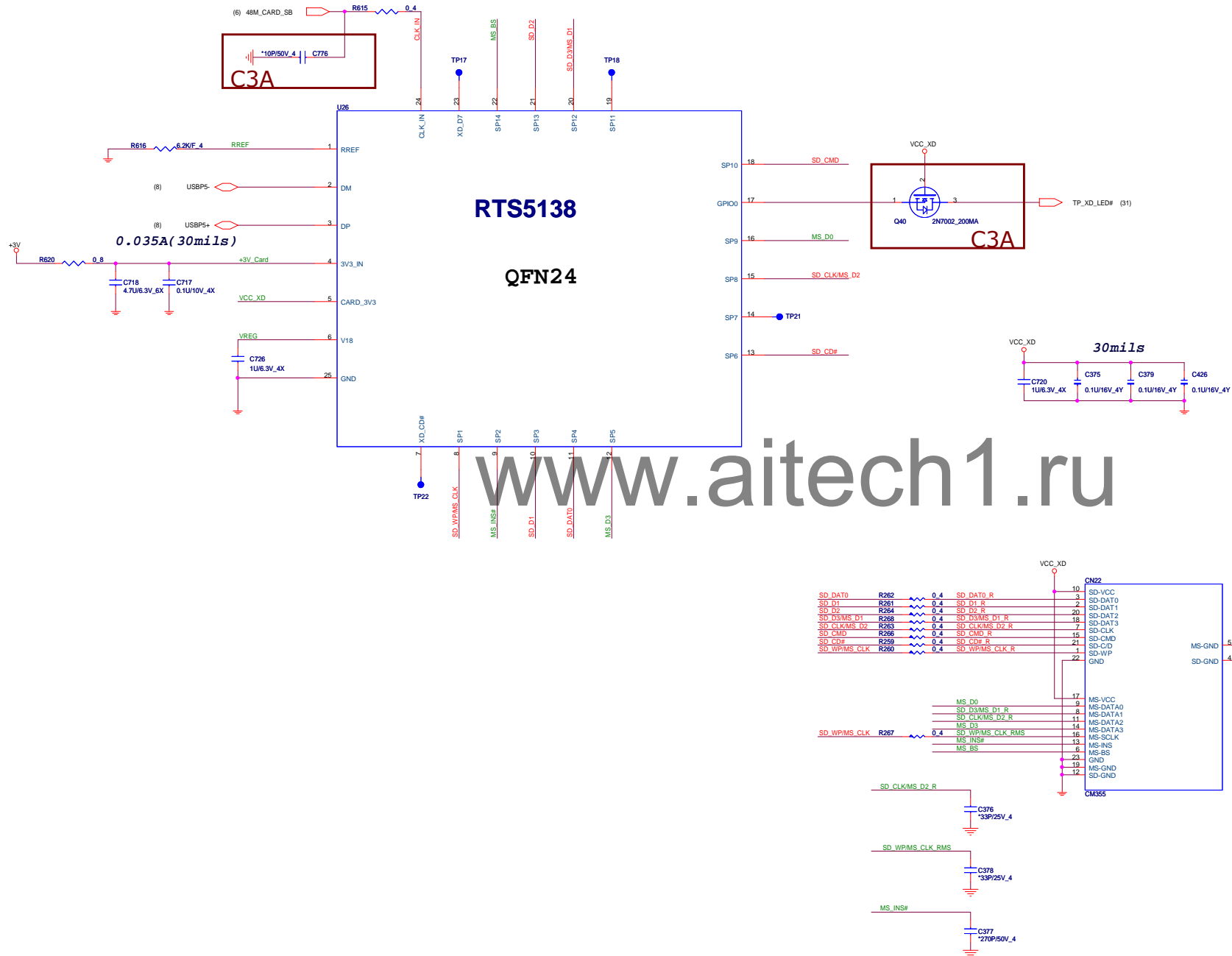


DG:EMI Requirement

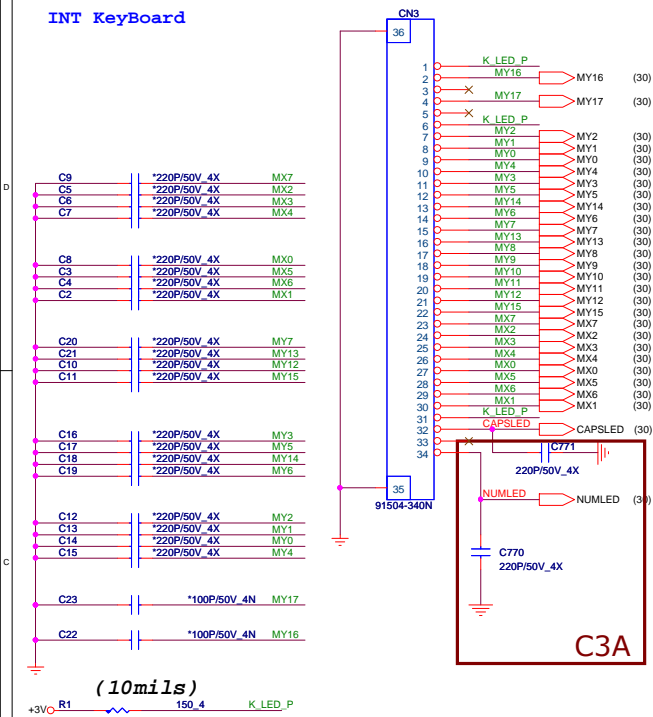


14" RJ45- DFTJ08FR164
15" RJ45- DFTJ08FR169
Transformer- DB0EL5LAN02

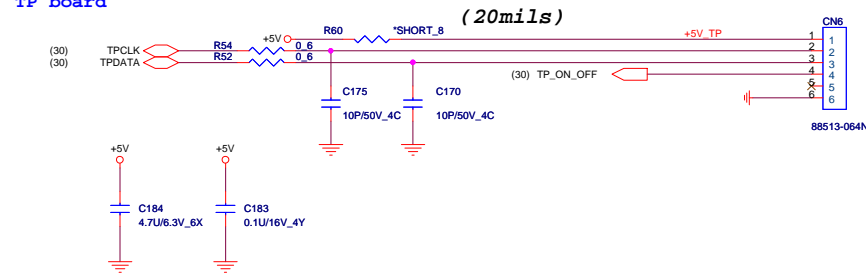
3 IN 1 CARD READER



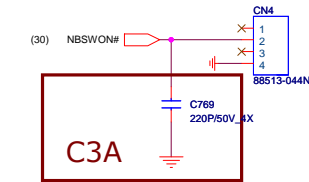
INT KeyBoard



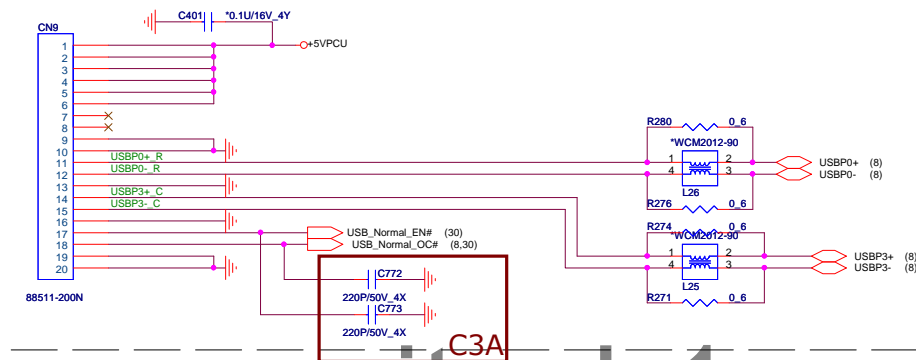
TP board



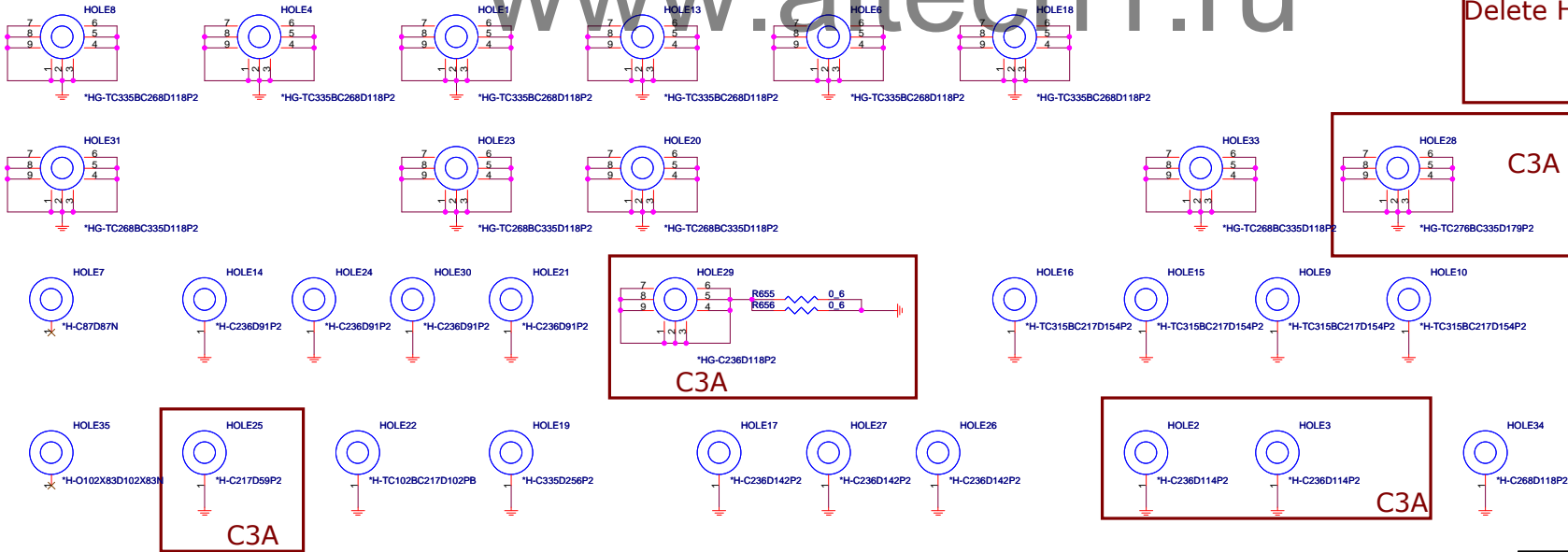
Power board



USB board



HOLE



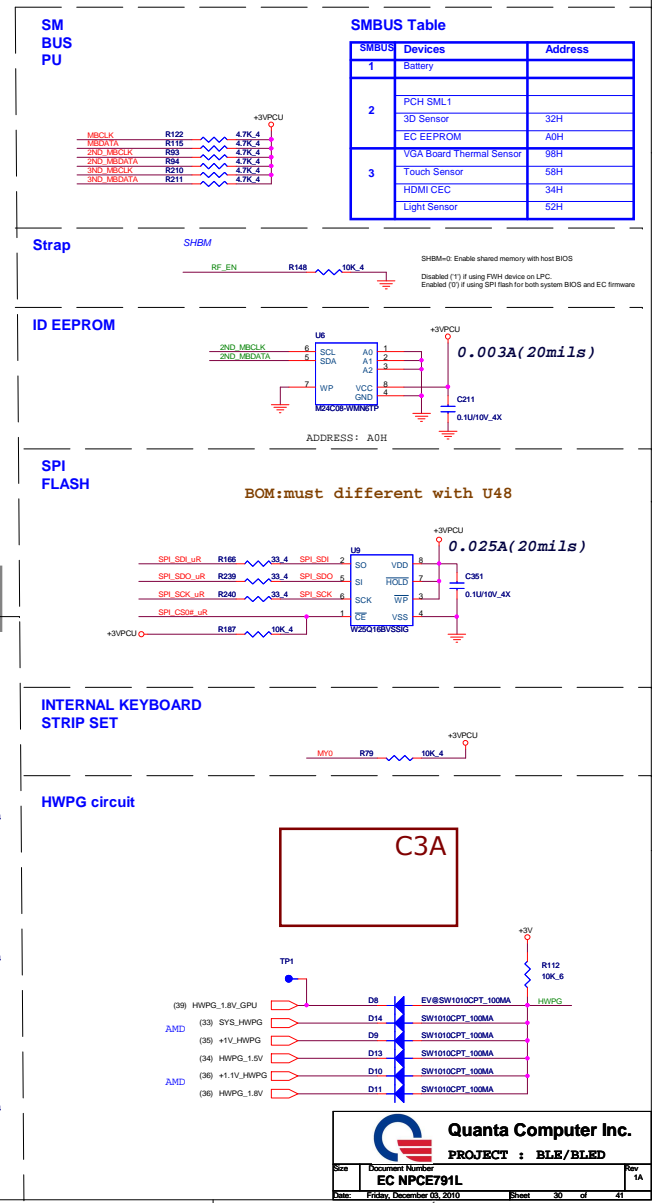
Delete Hole5, Hole12

C3A

C3A

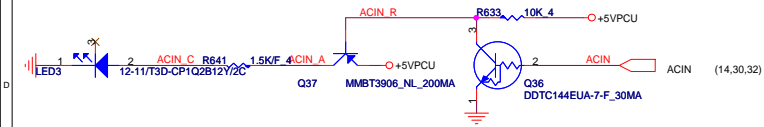
C3A



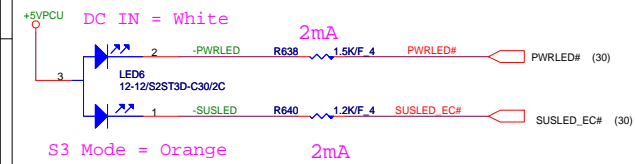


LED

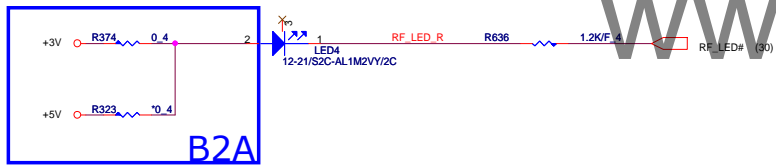
AC-IN



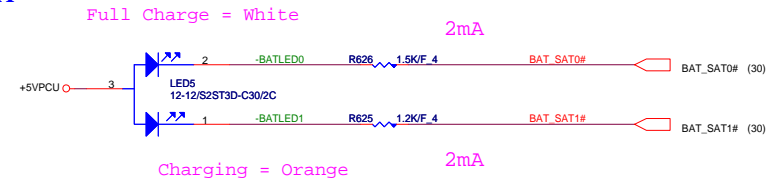
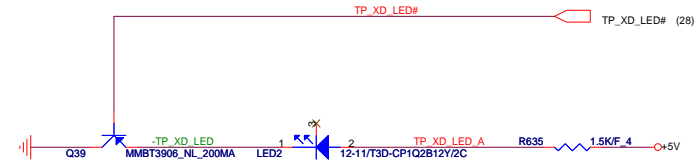
POWER



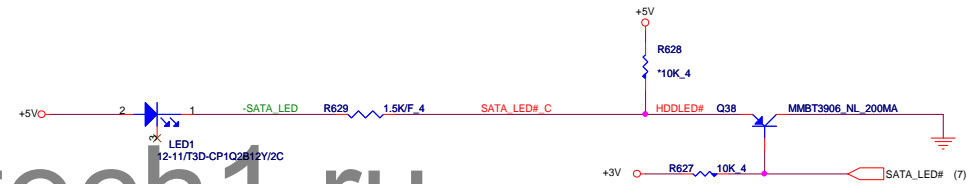
RF LED



BATTERY

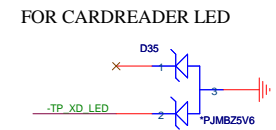
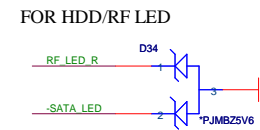
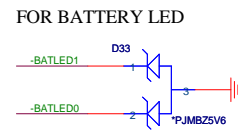
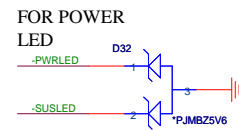
**CARDREADER**

HDD/ODD

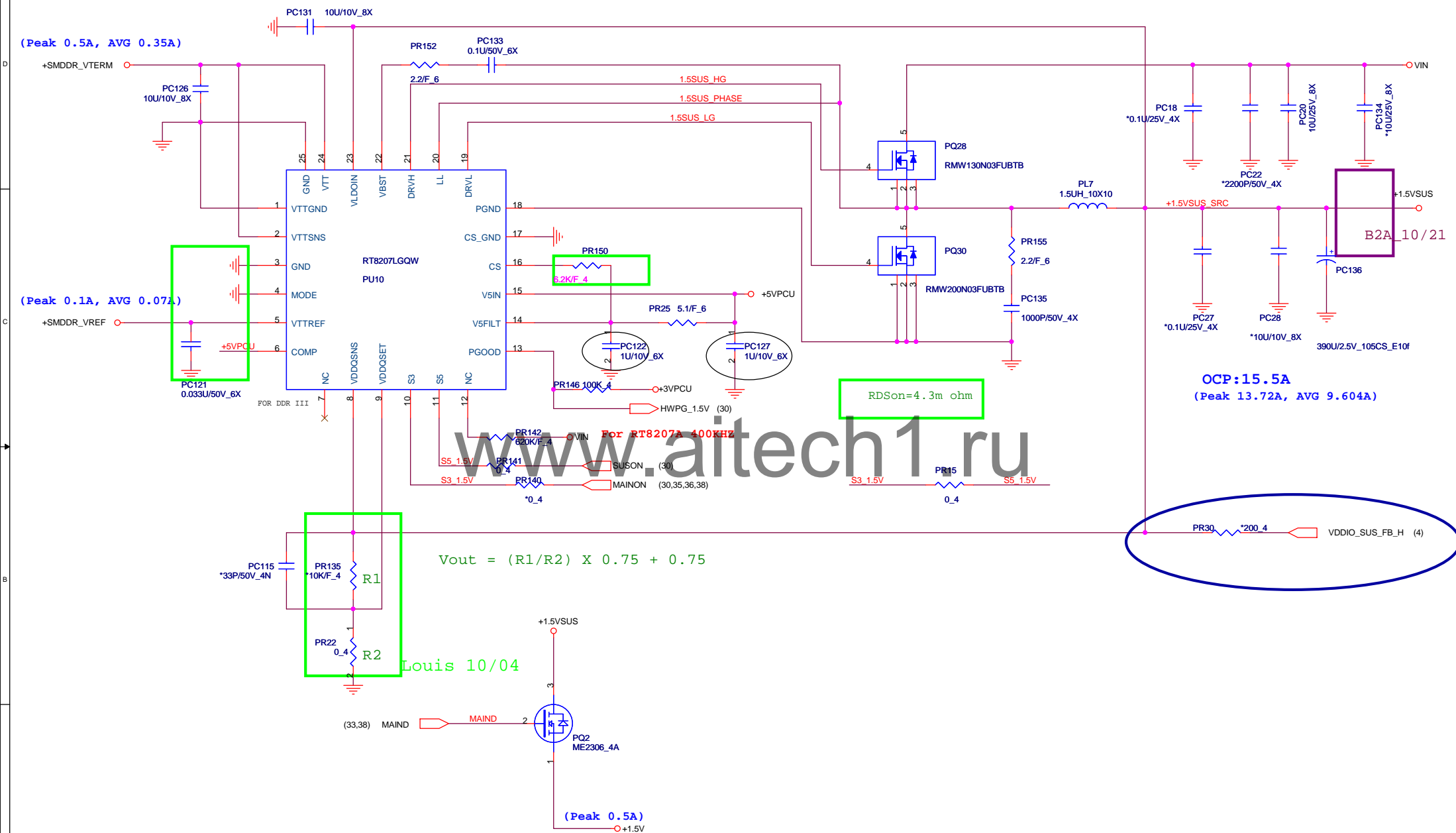


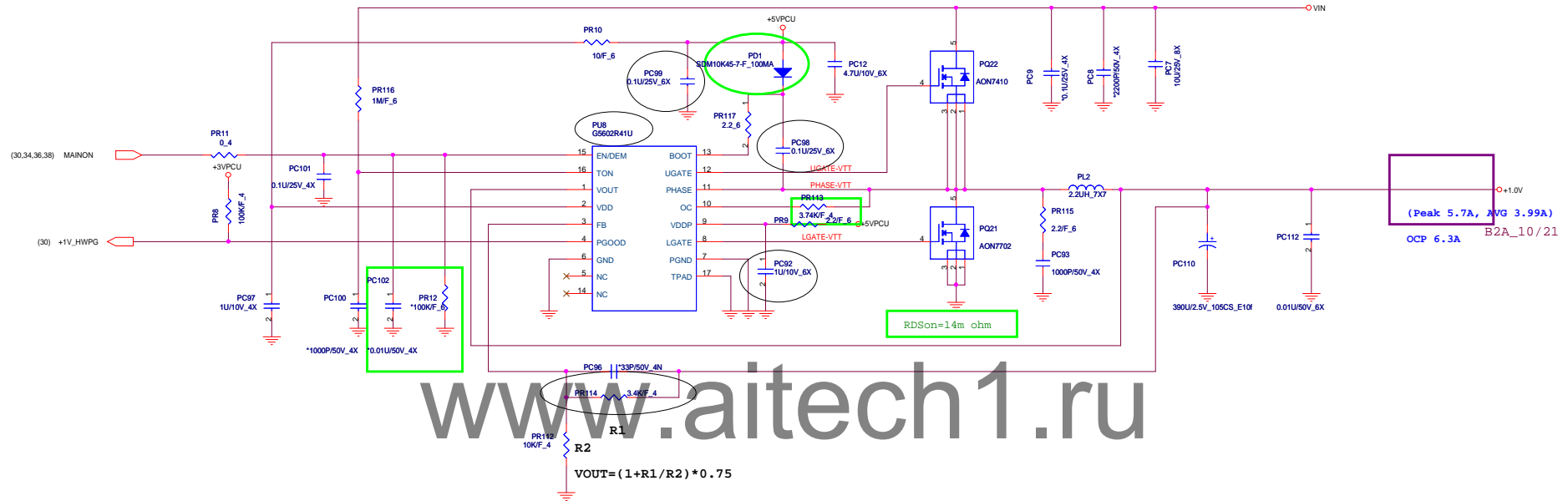
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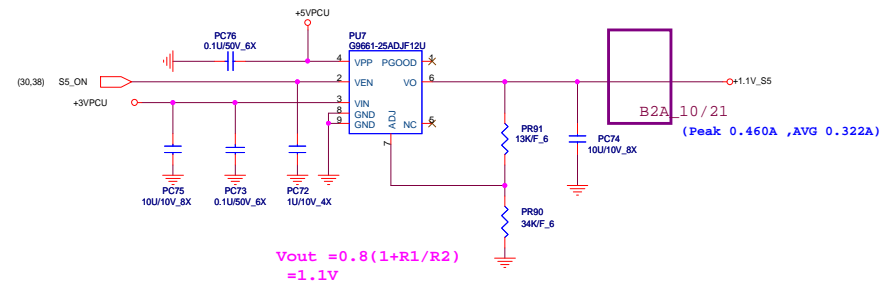
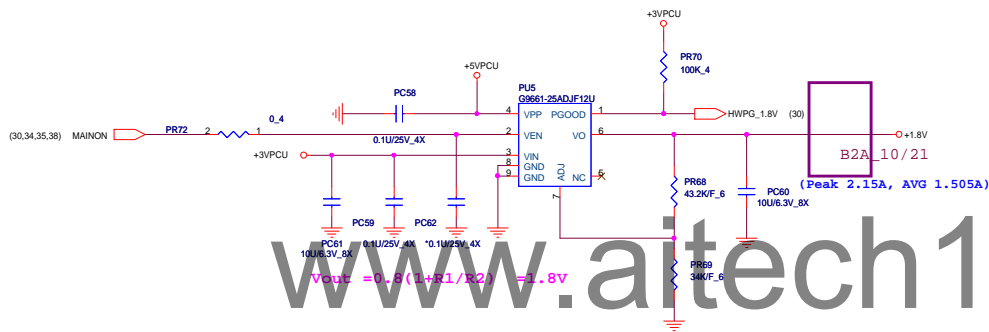
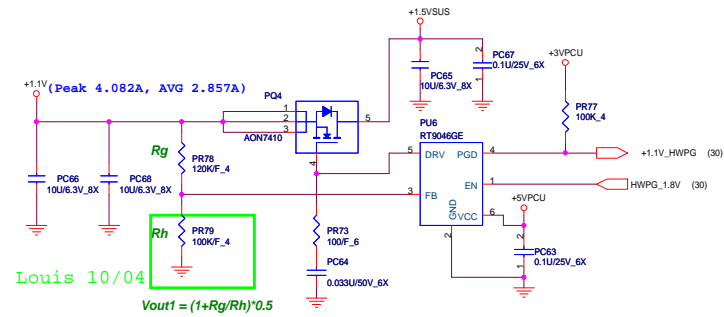
ESD Protect

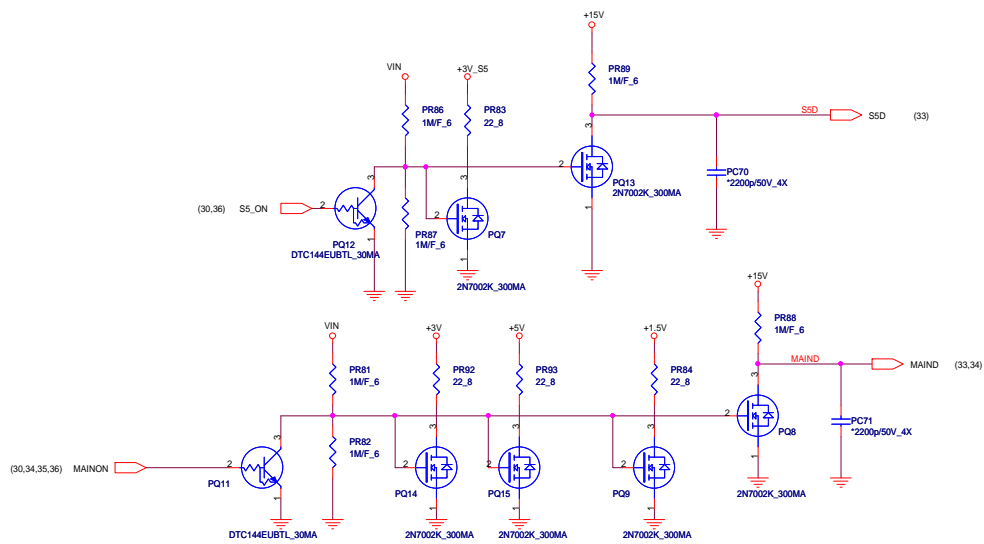






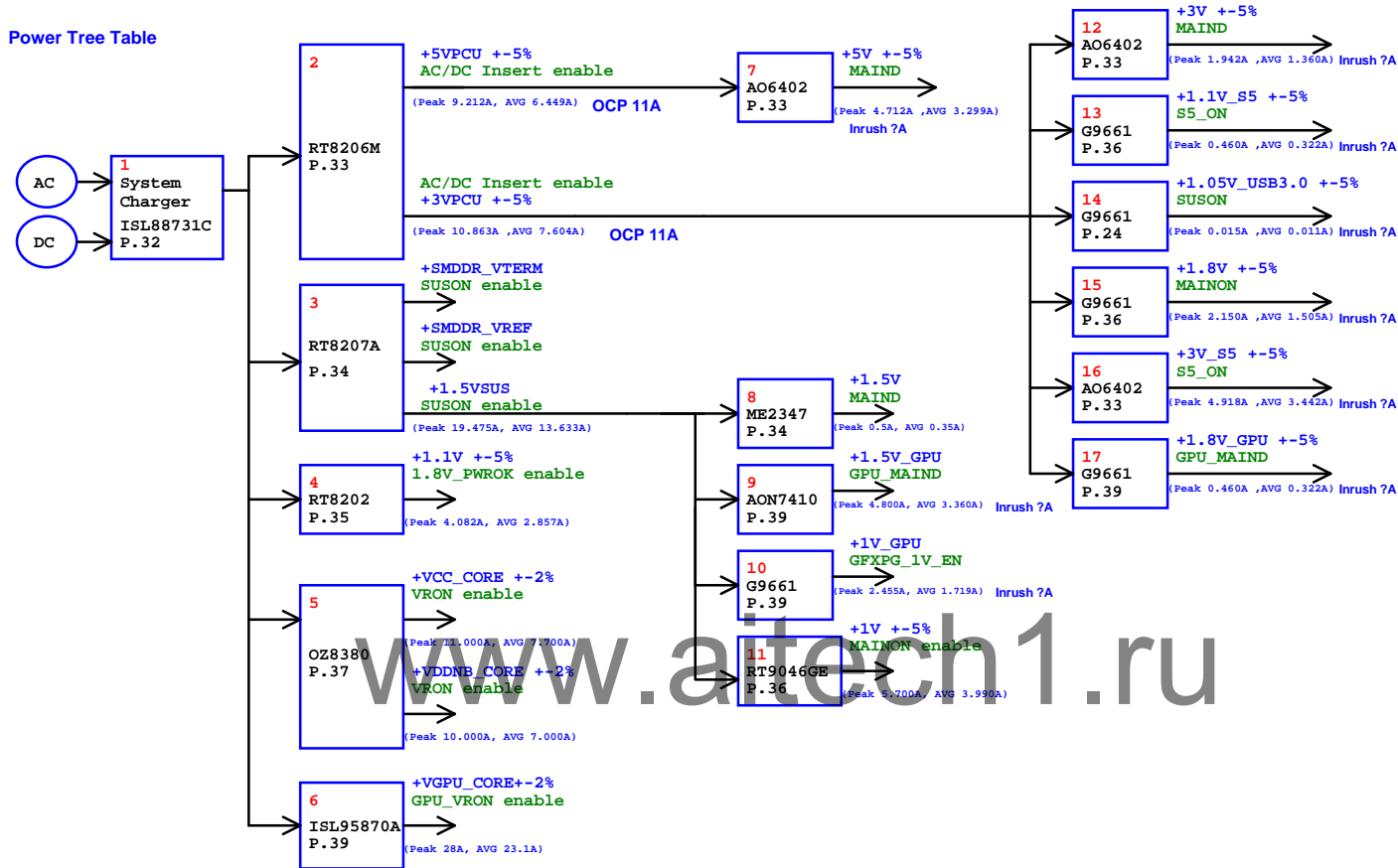






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Power Tree Table



Power Distribution List

Power	Distribution

Model	REV	CHANGE LIST	MODEL BLE/BLED							
			PAGE	FROM	To					
BLE/BLED MB		PAGE4: Remove R359, stuff R360	1	1A						
		PAGE8: Add R570 and G4	2	1A						
		PAGE21: Add C729,C732,C733,C734,C735,C736,C737,C738,C739,C740	3	1A						
		PAGE23: Stuff Q8 and remove R76	4	1A	2A					
		PAGE24: Add R642,R643	5	1A						
		PAGE26: Change C721,C410,C684 footprint to ShorTpac	6	1A						
		PAGE31: Add R374, reserve R323	7	1A						
		PAGE33: Add Pd11, PRI71, PRI70	8	1A	2A					
		PAGE33: 34, 35, 36, 37, 39: Remove power jumper PJP1-PJP9	9	1A						
		PAGE30: Delete R153, D15.	10	1A						
		PAGE8: Add R639	11	1A						
		PAGE28: Add Q40	12	1A						
		PAGE24: update CN16 footprint to usb-020053gr009m5126r-9p-smt	13	1A						
		PAGE30: ADD R644, R645	14	1A						
		PAGE32: change PL3,PL4 footprint to cc0805, need install components in C for EMI requirement.	15	1A						
			16	1A						
			17	1A						
			18	1A						
			19	1A						
			20	1A						
			21	1A	2A					
			22	1A						
			23	1A	2A					
			24	1A	2A					
			25	1A						
			26	1A	2A					
			27	1A						
			28	1A						
			29	1A						
			30	1A						
			31	1A	2A					
			32	1A						
			33	1A	2A					
			34	1A	2A					
			35	1A	2A					
			36	1A	2A					
			37	1A	2A					
			38	1A						
			39	1A	2A					
			40	1A						
			41	1A	2A					
DOC NO. 204			PROJECT MODEL :			BLE/BLED	APPROVED BY:		DATE:	
			PART NUMBER:				DRAWING BY:		REVISION:	2A